WAVEFORM GENERATOR FOR (EM) LOCATION OF TRAPPED MINERS

FINAL REPORT

JULY 14, 1974

PREPARED FOR
BUREAU OF MINES
U. S. DEPARTMENT OF THE INTERIOR
UNDER CONTRACT H0133045

COLLINS RADIO GROUP ROCKWELL INTERNATIONAL
TELECOMMUNICATIONS DIVISION
CEDAR RAPIDS, IOWA

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FOREWORD

This report was prepared by Collins Radio Group Rockwell International, Cedar Rapids, Iowa, under USBM Contract No. H0133045. This contract was initiated under the the Coal Mine Health and Safety Research Program. It was administered under the technical direction of the Pittsburgh Mining and Safety Research Center with Dr. H. K. Sacks acting as the technical project officer. Mr. Frank Pavlich was the contract administrator for the Bureau of Mines.

This report is a summary of the work recently completed as part of this contract during the period June 23, 1973, to July 23, 1974.

INTRODUCTION

USBM Contract H0133045 consists of the design, build and test of 50 waveform generators. The waveform generator is a small ULF transmitter operating in the 1 to 3 KHz frequency range for the purpose of locating trapped miners during a mine disaster.

This contract provided for the design, test, and building of 50 waveform generators using a discrete component construction with an option of using hybrid construction techniques within 105 days after the effective date of the contract. Because of large quantity economic considerations, this option was not initiated. Two engineering models were designed, constructed and tested and 50 final production units were fabricated using discrete construction. Complete documentation is supplied under a separate package which includes final schematics, parts list, layout information, equipment specification, production test procedures and qualification test procedures. Ten units have been delivered to the USBM. The remaining 40 units are being retained for packaging under contract H0242010 Transmitter Package and Receivers.

A great deal of experience has been gained as a result of this contract. A final discrete potted printed circuit configuration has been arrived at that is now ready for field testing. After field testing, any desired changes should be incorporated into a final design. However, as a result of the current experience gained building and testing the production units, this printed circuit package together with potting procedure could be improved to reduce future costs. For example, the printed circuit board could be increased in size by 0.125 to 0.2 inches and all components could be mounted directly to the board eliminating costly hand stacking of components. The new printed

circuit board would be potted in the mechanical package eliminating separate potting of the waveform generator and its' associated mold. Because the mechanical package would be the mold for the printed circuit, no overall size increase will be needed for the mechanical package the miner will eventually wear.

However, if any additional circuitry is added to the overall package a miner is required to wear, the decision to thin or thick film must again be examined. For example, should a down-link receiver be required, this circuit along with low level portions of the transmitter could be incorporated in thin or thick film circuits for both an economic and size advantage.

The information in this report covers the electrical and mechanical design aspects of the waveform generator and concludes with recommendations.

1.0 Electrical Design

1.1 Bridge Output Stage

The initial design for the bridge output stage is shown in Figure 1. This bridge was tested extensively and provided 7.0 amperes R.M.S. into a .2 ohm 100 UHY tuned antenna and 4.7 amperes R.M.S. into a .4 ohm 200 UHY antenna. This bridge is the best configuration for minimum saturated transistor drops, but untuned antennas and off resonance conditions resulted in transients that caused turn on of two transistors resulting in a short across the battery. This reduced the output current and placed an additional drain on the battery. To eliminate this problem the bridge configuration of Figure 2 was selected for the final design.

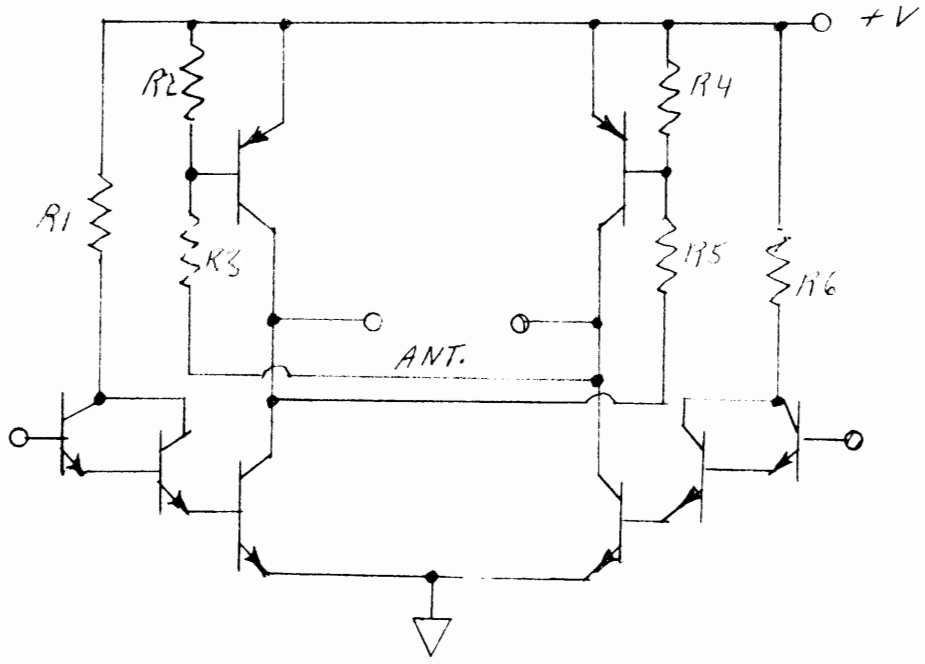

Figure 1 Initial Bridge Design

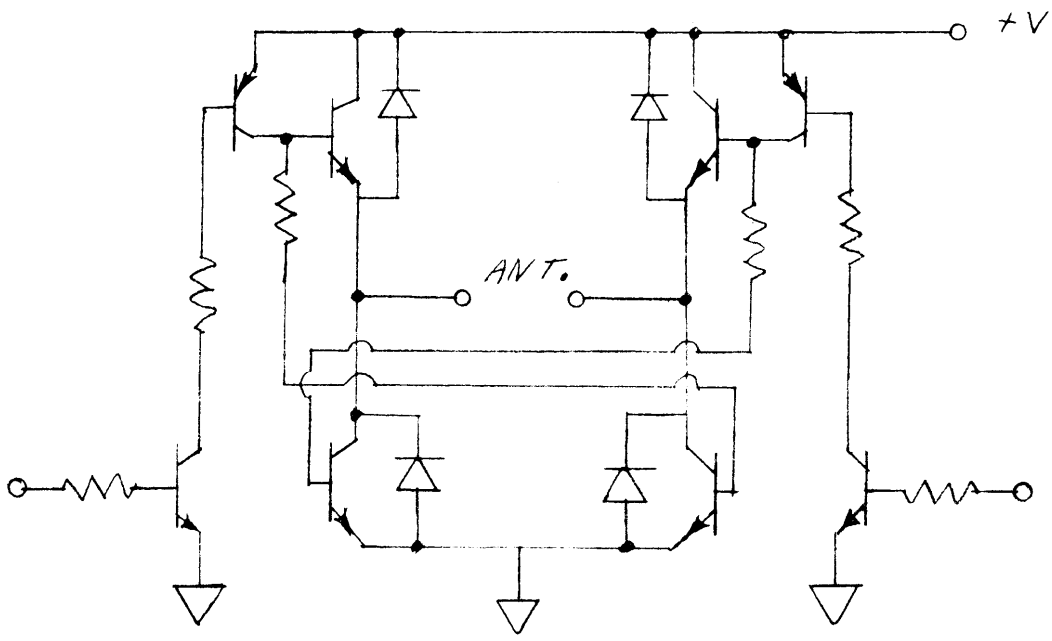

Figure 2 Final Bridge Design

This bridge does not have any tuning problems and returns energy back to the battery through the C-E diodes during off resonance switching for untuned loads. The RMS current is 5.7 amperes into a .2 ohm tuned 100 UHY antenna. R.M.S. current from -30°C to +60°C is not less than 5.6 amperes. The bridge can be operated continuously with a shorted or open antenna.

1.2 MOS Bridge Driving Circuitry

The drive logic for the bridge circuit consists of low power MOS inverter and nand gates. The logic required is to drive one side of the bridge high while driving the other side of the bridge low.

1.3 Crystal Oscillator

The crystal oscillator circuit shown in Figure 3 is a conventional pierce oscillator using a watch type quartz crystal.

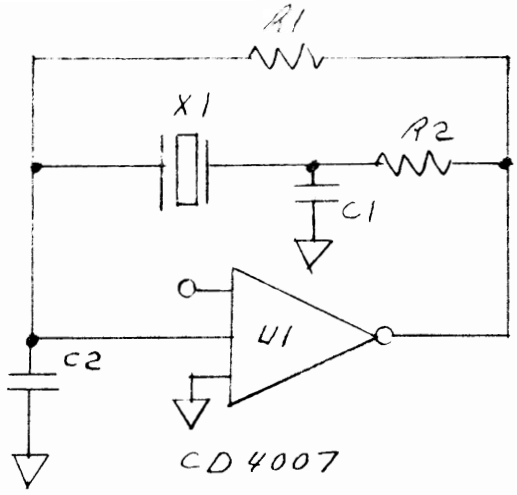

Figure 3 Crystal Oscillator Circuit

Resistor R1 biases the CD4007 in the linear range. It is large (22 megohms) so it doesn't affect the phase of the feedback network. Resistor R2 and capacitor C1 provide phase shift and limit the drive to the crystal. Capacitor C2 provides the proper input drive level for the circuit. Resistor R2 is changed to accomodate the frequency range of 33.6 KHz to 62.4 KHz. The 1050 Hz to 3030 Hz output is obtained by dividing down by 16 or 32 with the MOS divider CD4024. This circuit has been tested from -30°C to +60°C with less than 1 Hz variation at the 1 to 3 KHz output. A statek type SX-IV crystal is specified. An alternate crystal is available from McCoy that would work with some electrical and mechanical changes. An application note covering this oscillator circuit is attached to this report. The output frequencies have been assigned channel numbers. Beginning with 30 Hertz as channel 1. The output frequencies in Hertz can be determined by:

F = (Channel No.) x 60 - 30

The frequencies and channel numbers supplied under this contract are:

Channel	Frequency	Qty.
18	1050 Hz	10
26	1530	10
33	1950	10
43	2550	10
51	3030	10

All of the 34 channels assigned are tabulated in the equipment specification contained in the documentation package.

1.4 Duty Cycle Generator

The duty cycle generator shown in Figure 4 provides the gating for the 100 millesecond on time and .9 second off time. R3 + R4 and C3 provide the long off time constant. R4 and C3 provide the short on time constant. Temperature and voltage tests on the engineering model resulted in less than 3% variation in duty cycle from -20°C to +60°C and from 3.5 to 4.5 V.D.C. The duty cycle of some of the 50 units have been altered for experimentation purposes. If further field testing indicates a desired change of the duty cycle, it can be accomplished by changing R3, R4 and C3. It would not be desireable to change the per cent duty cycle to a larger value because this would increase the power dissipated in the unit.

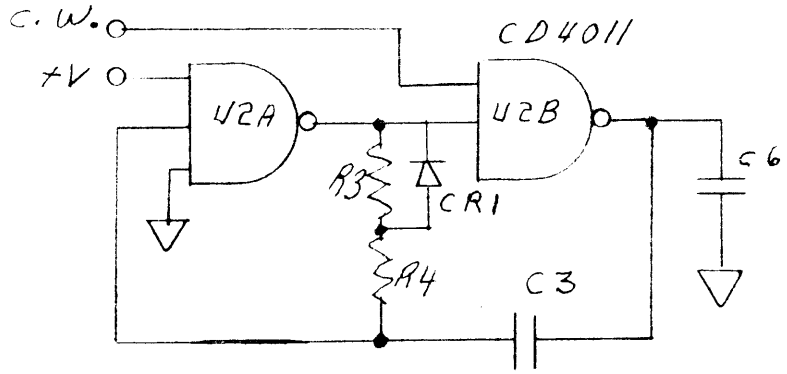

Figure 4 Duty Cycle Generator

1.5 Thermal

The output bridge driving 7.5 amperes into a .2 ohm resistor with a 10% duty cycle results in junction temperatures below 110°C. The maximum rated transistor junction temperature is 150°C. For safe reliable operation a derating factor of 75% is desirable and is attained in this design. If the initial duty cycle of 20% was retained the thermal design would be marginal.

The method of obtaining good heat transfer from the transistor case to the printed circuit board is by plating on the circuit board and tying this plating to the outer plated layers of the board. A thermal conductive epoxy bond is used between the transistor collectors and the printed circuit board.

1.6 Intrinsic Safety

The waveform generator has been designed in accordance with intrinsic safety guidelines. The waveform generator by itself is intrinsically safe and has been tested at the USBM for intrinsic safety. The waveform generator in combination with certain inductive antenna loads can be unsafe. The determination of safe antenna loads will be accomplished under contract H0242010 Waveform Generator Package and Receivers.

1.7 Battery Life

Life tests with the original bridge resulted in operating life of greater than 12 hours. A battery was fully charged and then operated with a cap lamp load for 8 hours. The cap lamp was turned off and the waveform generator was connected to the battery. The antenna load was a tuned 100 UHY antenna (.2 ohms D.C.R.) the R.M.S. current was as follows:

Time	Current
turn on	5.1 Amps R.M.S.
5 hours	4.9
12 hours	4.2

The unit was turned off overnight (12.5 hours). The next morning it was turned on with an initial current of 4.2 amperes. After 3 hours of operation the current was 2.1 amperes. At this time the battery was essentially dead.

Later tests with the final bridge configuration resulted in operating times of greater than 24 hours. The final bridge configuration results in longer life because of slightly reduced output current and transistor drive power. Under the same conditions as before results are

as follows:

Time	Current
turn on	4.52 Amps R.M.S.
9 hours	3.54
11 hours	2.83
14 hours	2.26
19 hours	2.12
24 hours	1.98

Results of another life test under the same conditions are as follows:

Time	Current
turn on	4.95 Amps R.M.S.
4 hours	4.95
16 hours	4.5
20 hours	4.24
24 hours	3.7
28 hours	3.6

The variation of current shown in these last two life tests is due mostly to different batteries, although per cent duty cycle, tuning, and the amount of time the unit was run continuously during measurements are also factors. Life tests were run using batteries that were approximately 1 year old, but essentially new with less than 10 charge cycles.

From these life tests is appears that adequate operating time is available for location during an emergency. These operating times will be extended in actual field use since the defined antennas are now not less than .4 ohms (D.C.R.) A 20% increase in life can be expected.

For information concerning battery characteristics with age, the following data is presented for three batteries obtained from MSA that were ready for discard.

Unit	1	2	3
Internal R	.101Ω	.113Ω	.101Ω
Cap Lamp Life	5 hrs.	7 hrs.	8 hrs.
No Load Voltage	4.09V	4.04V	4.23V
Cap Lamp Load Voltage	3.89V	3.88V	4.02V

1.8 Antennas

The initial specified load for the waveform generator was .2 ohms D.C.R. and a 100 UHY inductor. The present defined antennas are the 90 foot of #16 portable antenna which is *47 UHY (.36 ohm D.C.R.) and the 400 foot #10 fixed antenna which is 233 UHY (.4 ohm D.C.R.). A lot of the testing of the waveform generator has been done using the .2 ohm antenna which is much more than a worst case condition as far as power dissipation, battery life etc. is concerned. In general the waveform generator has been operated more severely than will be required in actual field use.

*Calculated from N.B.S. circular C-74.

2.0 Mechanical Design

The initial package size objective was 1.3 x 1.3 x .5 inches. With an option at 105 days ARO to go to a hybrid package. At this time four approaches became apparent. A two layer package 1.3 x 1.5 x .5 inches, a single layer 1.3 x 3.25 x .25 inches, a thin film 1.25 x 1.25 x .5 inches and a thick film 1.25 x 1.25 x .5 inches.

Considering cost, technical risk and heat conduction the decision was made to use the single layer 1.3 x .3 x 3.25 inch discrete approach. Budgetary costs are shown in Table I.

The 1.3 x 3.25 x .3 inch package is potted with a sylgard compound for water proofing, resulting in a final size of 1.4 x .35 x 3.45 inches. The potting process with a single mold has proven to be troublesome, time consuming and expensive so that future builds should consider placing the circuit board into the transmitter package cavity and then pouring in the potting material.

Electrical connections from the waveform generator consist of five 6-inch #20 bus wires with teflon sleeving. The package has been operated while immersed in water with no problems. A picture of the unpotted and potted waveform generator is shown in Figure 5 and 6.

WAVEFORM GENERATOR BUDGETARY COST ESTIMATES

PROCESS	QUANTITY					
	200	1K	5K	10K	50K	100K
DISCRETE (TWO STACKED BOARDS)	74.36	47.47	43.04	39.17	36.35	36.79
DISCRETE (SINGLE BOARD)*	70.42	44.47	40.04	36.67	34.35	34.79
THICK FILM	166.53	65.67	60.11	54.17	51.61	47.60
THIN FILM	94.21	52.17	46.38	43.59	39.64	38.62

* Selected Process

TERMS AND CONDITIONS

FOB PLACE OF MANUFACTURER

THICK FILM: PRICE INCLUDES 6.5% TARIFF

DELIVERY: 200 QUANTITIES OVER 1 YEAR, 1000 THRU 10K QUANTITIES OVER 2 YEARS, AND ABOVE 50,000, OVER 3 YEARS.

THIN FILM: PRICE INCLUDES 30 BURN IN SOCKETS. ADDITION BURN IN SOCKETS $15 EACH.

TABLE I

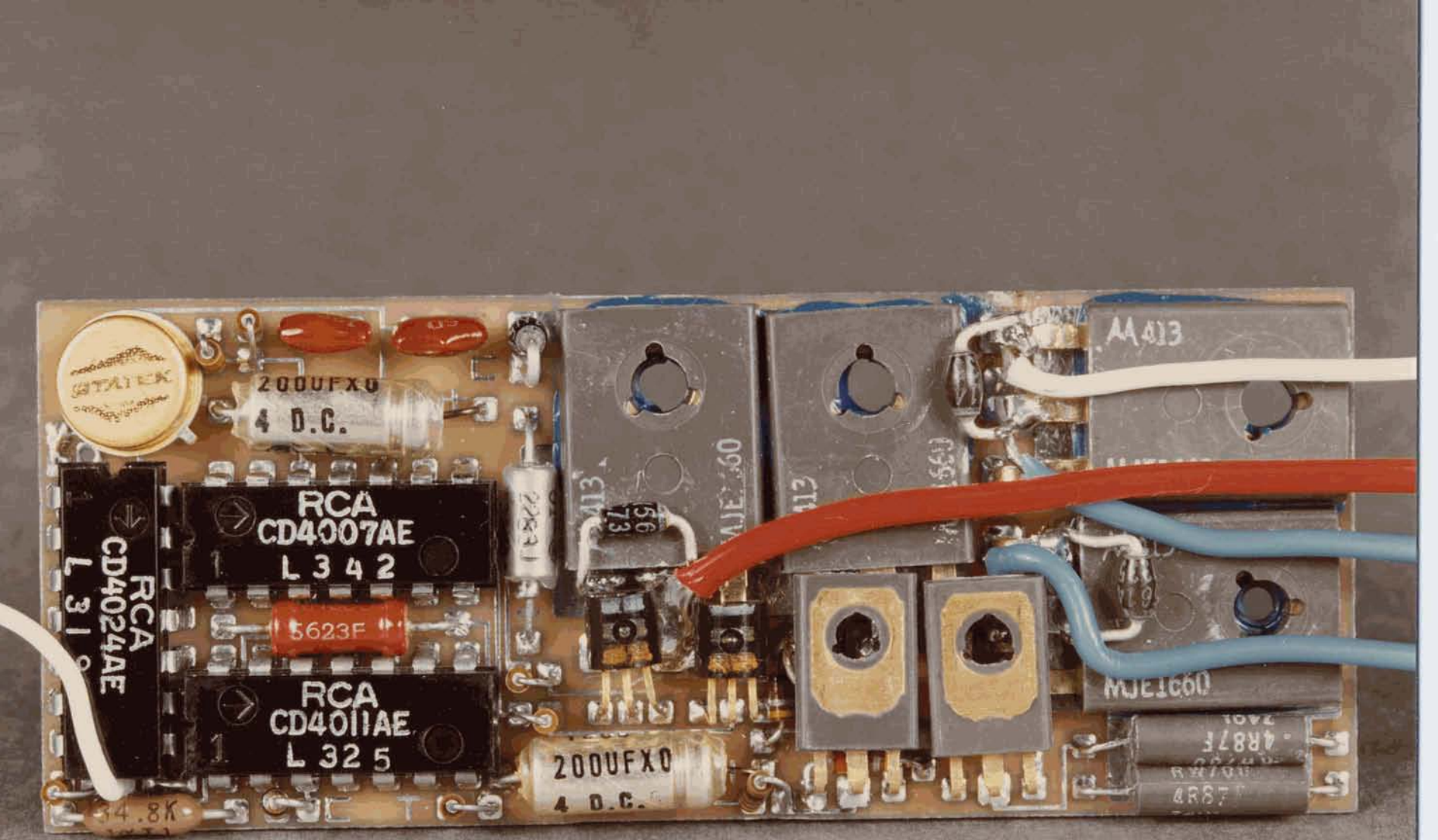

Figure 5
Waveform Generator
Circuit Board

Figure 6
Waveform Generator
Encapsulated

3.0 Problems

The experience gained from the production of 50 waveform generators has indicated that the C-MOS integrated circuits variation in production lots is a problem.

The C-MOS used for this contract is specified for operation from 3.0 to 15 volts. For logic operation such as the drive logic for the bridge circuit, the C-MOS operation is adequate. But for the linear operation such as in oscillator circuit and the duty cycle generator, the degradation of the transfer characteristic of some of the C-MOS at low voltages causes problems. A no start problem with a load connected before applying power has occured in some units and variation of the duty cycle on and off times is a problem in some units. For the build of 50, a capacitor was added to eliminate the no start problem and some selection of integrated circuits was necessary to control the duty cycle time.

For future builds the RCA TA-6178 low level (1.1 to 6 volts) C-MOS should be considered if it becomes a standard line and is available in production quantities. Also the new line of C-MOS by Fairchild has been tested and has a superior transfer characteristic at low voltages.

4.0 Recommendations

Because of low voltage problems, for future builds it is recommended that the RCA low voltage TA 6178 integrated circuit be used if it becomes available. Also, the Fairchild C-MOS should be used because of its superior transfer characteristic at low voltages. It is anticipated that eventually other C-MOS manufacturers will improve their C-MOS so that it may not be required to specify Fairchild C-MOS. The

potting process provides good water and humidity protection but should be modified so that the board is placed in the transmitter cavity and then filled with potting compound rather than potting each waveform generator in a separate mold. The separate or multiple mold process has proven to be time consuming and troublesome. Also, this would allow the board to be made slightly larger to facilitate direct placement of all components on the board to ease assembly rather than stacking some components as is done on the present board.

The waveform generator should now be tested in actual field use to determine if there are any desired changes. Future builds would require a modest amount of engineering to incorporate all of the above recommendations. With these final recommendations, the waveform generator will be a tested producible product.

APPLICATION NOTES FOR LOW POWER CRYSTAL CONTROLLED OSCILLATORS

This application note is intended to provide the engineer with a basic low power crystal oscillator design. Two examples using a CMOS inverter (CD 4007) controlled by a STATEK quartz crystal are illustrated, and the basis for selection of various components are given.

In the first example, Figure 1, complementary MOS is used in the oscillator and buffer amplifier of the circuit. The supply voltage V_{dd} must be sufficiently greater than the sum of the threshold voltages of the N- and P- channel MOSFETS to provide a bias current through the amplifier, thereby giving the unit sufficient gain to start and maintain oscillation. The circuit can be designed to operate with a voltage in the range of 3 VDC to 15 VDC. Although, consideration must be given in the design so as not to drive the crystal in excess of 2 volts peak to peak. Table 1 lists typical component values for operation of this circuit with supply voltages less than 9 VDC.

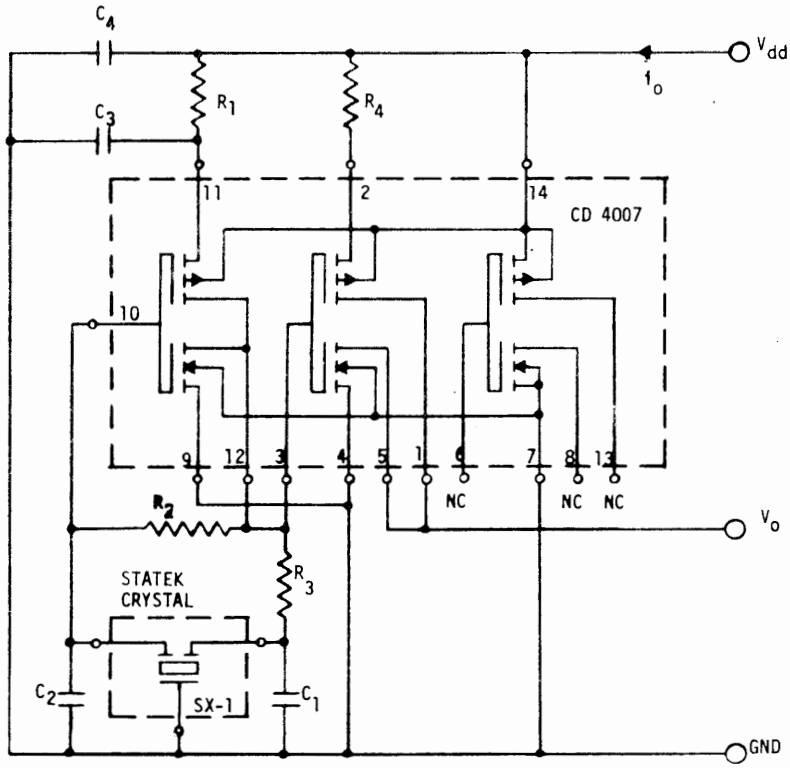

FIGURE 1 CMOS CRYSTAL OSCILLATOR
For Operation with a 3 to 9 Volt Supply

For operation with a supply voltage, V_{dd}, in the range of 5 to 15 volts the circuit in Figure 2 is recommended. In this example, an N-channel MOS-FET is used in the oscillator and the first stage buffer amplifier. A complementary MOS is used as the output stage of the buffer amplifier.

Frequency Range KHz	C_1 pf	C_2 pf	R_1 K ohm	R_2 M ohm	R_3 K ohm	R_4 K ohm
10-40	20	5	100	22	680	10
40-100	10	0	100	22	150	10

TABLE 1 TYPICAL VALUE OF COMPONENTS USED IN THE STATEK CMOS CRYSTAL OSCILLATOR

STATEK CORPORATION
1200 ALVAREZ AVENUE ■ ORANGE, CALIFORNIA 92668 ■ (714) 639-7810

In this circuit the crystal drive voltage is limited to 0.6 to 1.4V by R_3 and C_1. Within this voltage range the STATEK crystals will not be over driven. The supply voltage V_{dd} can be 5 to 15 volts for frequencies in the range of 10 KHz to 60 KHz, and 9 to 15 volts for frequencies over 60 KHz. Table 2 lists typical component values for use in this circuit. The average current for this design is given in Figure 3 for various supply voltages and operating frequencies.

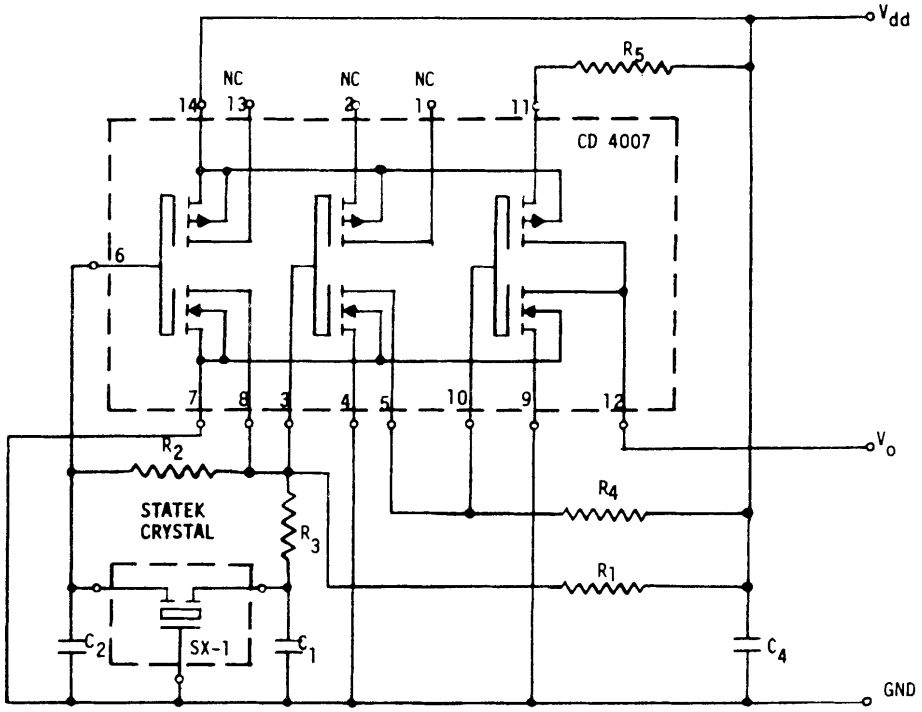

FIGURE 2 N-CHANNEL MOSFET CRYSTAL OSCILLATOR

For Operation with a 5 to 15 Volt Supply

Frequency Range KHz	C_1 pf	C_2 pf	R_1 K ohm	R_2 M ohm	R_3 K ohm	R_4 K ohm	R_5 K ohm
10-40	20	5	1500	22	500	220	10
40-100	10	0	500	22	150	86	10

TABLE 2 TYPICAL VALUE OF COMPONENTS USED IN THE STATEK N-CHANNEL CRYSTAL OSCILLATOR

A brief explanation of the function of each component in the example circuits is given below. The typical component values show the range used in optimizing the circuits for minimum current at various supply voltages.

(1) Resistor R_1, sets the gain of the amplifier in the oscillator, and determines the oscillator output voltage V_o and the crystal drive level V_d. It also reduces the oscillator current drain. The value of this resistor is 100 K ohm to 1.0 megohm for CMOS oscillator design (Figure 1), depending on the operating frequency and the supply voltage V_{dd}. In the N-channel oscillator design (Figure 2), R_1 is 500 K ohm to 1.5 Megohm depending on frequency and supply voltage.

(2) Resistor R_2, the bias resistor, must be large enough so as not to appreciably affect the phase of the feedback network, typically 20 Meg ohm or greater.

(3) Resistor R_3 is used to limit the crystal drive level while providing a voltage sufficient to drive the first stage of the buffer amplifier. It also provides the appropriate phase shift when the tank circuit is operated slightly below anti-resonance. R_3 should be approximately equal to X_{CL} with values ranging from 0 to 1 Meg ohm.

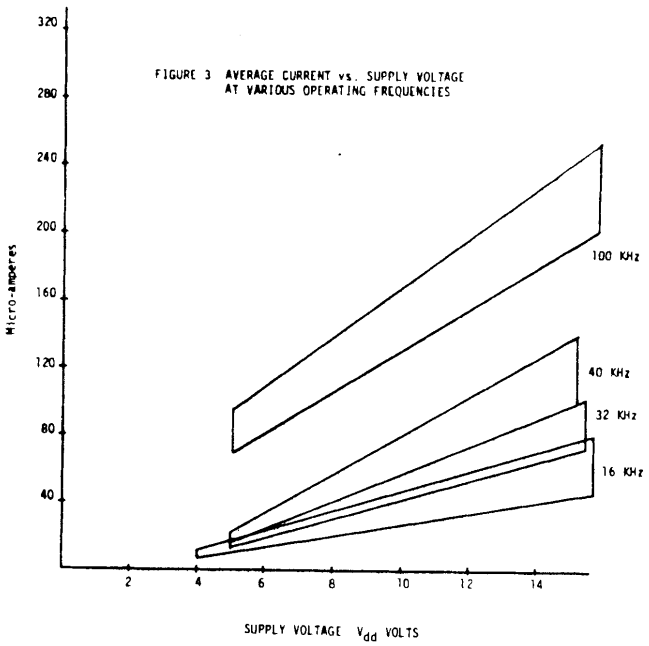

FIGURE 3 AVERAGE CURRENT vs. SUPPLY VOLTAGE AT VARIOUS OPERATING FREQUENCIES

(4) Resistors R_4 and R_5 determine the output voltage of the first and second stage buffer amplifiers, respectively, and limit the current in the buffer amplifiers. Their value must be large enough so the amplification stage will saturate and small enough so the amplifiers will have sufficient drive capability. R_4 in the CMOS oscillator, Figure 1, is typically one-tenth the value of R_1. In the N- channel oscillator, Figure 2, R_4 is typically 50 K to 300 K ohm. R_5 is typically 5 to 15 K ohm.

(5) Capacitor C_1 is used to determine the drive voltage V_d and also provides the appropriate phase shift in the feedback network, typically 10 to 100 pf.

(6) Capacitor C_2, determines the input voltage of the oscillator amplifier. Its value is optimized between frequency stability and gain, typically 0-20 pf.

(7) Capacitor C_3, the decoupling capacitor, is chosen in conjunction with R_1 to give an RC time constant which isolates the oscillator from low frequency noise, typically 0.01 to 0.1 microfarad in the CMOS oscillator design, Figure 1.

CIRCUIT THEORY

The basic configuration of both oscillator designs is commonly referred to as a Pierce circuit. In a Pierce oscillator the crystal and two capacitors, C_1 and C_2 from the feedback network.

The fundamental criteria governing this design is illustrated in Figure 4. For oscillation to occur the Barkhausen criteria must be met: (1) the loop gain must be greater than one; (2) the phase shift around the loop must be 360°.

For analyzing the design the equivalent electrical circuit of a quartz crystal is used. Figure 5 shows the electrical equivalent circuit of a typical STATEK quartz crystal. The L_m, C_m, and R_m are generally referred to as the electrically equivalent of the mechanical parameters inertia, restoring force and friction, respectively, and can be measured with a crystal impedance meter. The two branches of L_m, C_m, and R_m represent two modes of vibration: (1) is the fundamental and (2) is an overtone (approximately 6 times the fundamental frequency). C_S is capacitance between the electrodes on the top surface of the tuning fork, and C_{gs} is the geometric capacitance due to the quartz thickness and electrode area. This circuit can be simplified by the equivalent resistance and reactance of the crystal at frequency f which are designed as $R_e(f)$ and $X_e(f)$, respectively.

Figure 6a shows the AC equivalent circuit of the amplifier and feedback network of the Pierce oscillator. In this circuit g_m and r_d are the forward transconductance and output impedance of the amplifier. R_1 is the resistor used to determine the amplifier output or crystal voltage V_o. The sum of the output capacitive reactance of the amplifier, the input of the buffer amplifier and the external added capacitor for adjusting the proper phase relation between input

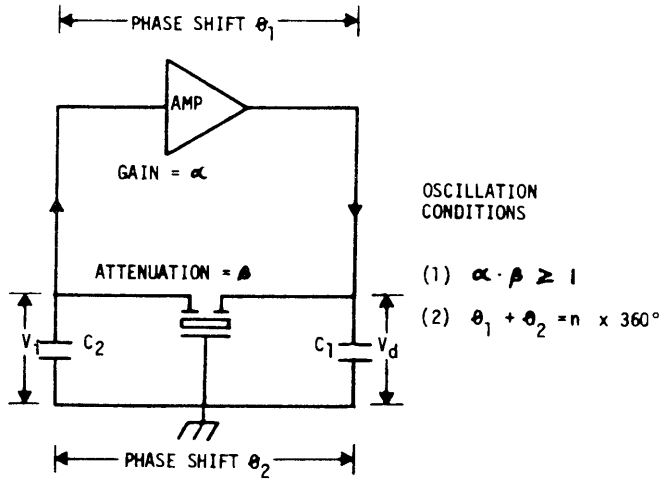

FIGURE 4 BASIC PIERCE OSCILLATOR

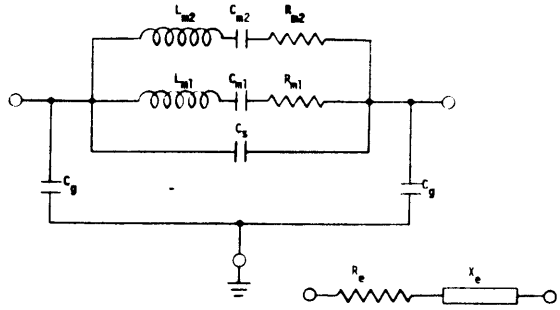

FIGURE 5 ELECTRICAL EQUIVALENT CIRCUIT OF STATEK QUARTZ CRYSTAL

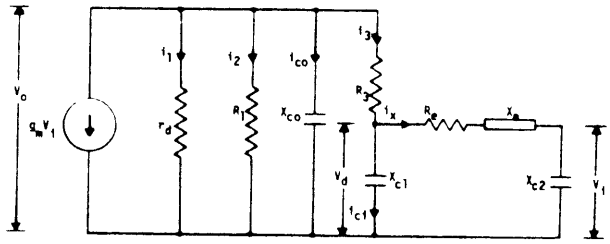

Figure 6a AC EQUIVALENT CIRCUIT OF PIERCE OSCILLATOR

and output voltage of the amplifier is represented by X_{co}. Resistor R_3 is used to limit the crystal drive level while providing sufficient output drive voltage to a buffer amplifier stage. In order to obtain the maximum transfer ratio between the input and output voltage of the feedback network, the tank circuit, i.e. the arm of X_e, R_e, X_{C2} in parallel with X_{C1}, must be near anti-resonance. Under this condition the current flowing through the crystal will be maximum. To satisfy the anti-resonant condition, the following equations must be fulfilled:

$$X_{C1} = [R_e^2 + (X_e - X_{C2})^2] \Big/ (X_e - X_{C2})$$

and $X_e - X_{C2}$ must be inductive. The operating frequency (f_o) will, therefore, be slightly greater than the series resonance frequency of the crystal (f_s) and can be approximated by

$$f_o = f_s \sqrt{1 + \frac{C_m}{C_t}} \quad ,$$

where C_m is the motional capacitance of the crystal, which is of order of 10^{-3} pf, C_t is the capacitance of the series combination of C_1, C_2 and C_g. The latter is on the order of 1 pf. The operating frequency (f_o), therefore, can be tuned by adjusting the value of C_1 or C_2.

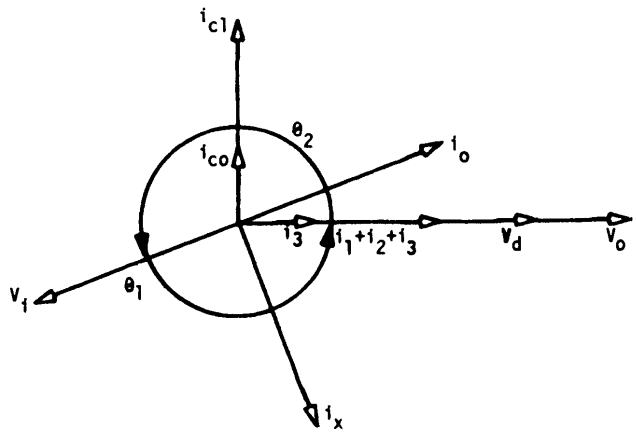

FIGURE 6b THE PHASE RELATION BETWEEN CURRENTS AND VOLTAGES IN THE OSCILLATOR CIRCUIT

For this circuit the phase relation between the crystal current, driving voltage and output voltage is shown in Figure 6b. The input voltage of the amplifier lags the current i_x by 90° since the input resistance of CMOS is relatively high. In general, under this condition the phase shift θ_2 for V_o to V_i through the feedback network is larger than 180°. The phase angle between input voltage V_i and the amplifier output current i_o is 180°. With an approximate X_{co}, the phase angle θ_1 between input voltage V_i and output voltage V_o through the amplifier will be 360° - θ_2.

The transfer ratio of V_1 to V_o through the feedback network is

$$\beta = \left| \frac{V_i}{V_o} \right| = \frac{(X_e - X_{C2})^2 + X_{C2}^2 R_e^2}{R_3 R_e + R_e^2 + (X_L X_{C2})^2}$$

and the phase angle is

$$\theta_2 = \tan^{-1} [R_e / (X_e - X_{C2})]$$

The gain of the amplifier α is approximately equal to $g_m Z_L$

$$\alpha = \left| \frac{V_o}{V_i} \right| \approx g_m Z_L$$

where Z_L is the total impedence across the drain to the source. The phase angle θ_1 is then

$$\theta_1 = \tan^{-1} [(\text{Imag.} Z_L) / (\text{Real } Z_L)]$$

The conditions for the oscillation are

$$\alpha\beta \geq 1$$

and $$\theta_1 + \theta_2 = n\ 360°$$

NOTES: