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CMOS Amperometric ADC with High Sensitivity, Dynamic Range and Power Efficiency for Air Quality Monitoring

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Abstract

Airborne pollutants are a leading cause of illness and mortality globally. Electrochemical gas sensors show great promise for personal air quality monitoring to address this worldwide health crisis. However, implementing miniaturized arrays of such sensors demands high performance instrumentation circuits that simultaneously meet challenging power, area, sensitivity, noise and dynamic range goals. This paper presents a new multi-channel CMOS amperometric ADC featuring pixel-level architecture for gas sensor arrays. The circuit combines digital modulation of input currents and an incremental ΣΔ ADC to achieve wide dynamic range and high sensitivity with very high power efficiency and compact size. Fabricated in 0.5 μm CMOS, the circuit was measured to have 164 dB cross-scale dynamic range, 100 fA sensitivity while consuming only 241 μW and 0.157mm^2 active area per channel. Electrochemical experiments with liquid and gas targets demonstrate the circuit's real-time response to a wide range of analyte concentrations.

Index Terms

Amperometric; sensor array; wide dynamic range; high sensitivity; sigma delta (ΣΔ) ADC

I. Introduction

Exposure to airborne pollutants causes many diseases such as lung cancer and respiratory infections [1, 2] and consistently ranks among the leading causes of mortality globally. The lack of effective preventative measures and treatments are due in large part to our inability to properly characterize and quantify acute exposure to air pollutants, and thus a portable/wearable ambient gas sensor array could effectively improve human health by monitoring personal exposure to air toxins.

Electrochemical sensing is a promising modality for a wearable air quality monitoring system due to its extremely low cost and power consumption, suitability for miniaturization, and high sensitivity and selectivity. Many electrochemical sensors are operated with a technique known as chronoamperometry [3–5], in which the sensor is stimulated by a constant DC potential and generates a response current that correlates with the concentrations of one or more target compounds. Using amperometry methods, an electrochemical sensor's bias potential can be tuned to a point of maximum reactivity with a

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specific gas, and sensor arrays at multiple bias potentials can be employed to statically calibrate for interferents and improve selectivity using pattern recognition algorithms [6]. Many amperometric gas sensors are both commercial and academically available for measuring O_2, CO_2, NO_x, CO, SO_2, H_2S and volatile organic compounds (VOCs), which affect human health [6–9]. The versatility of this technology suggests that an array of electrochemical sensors can simultaneously measure the concentration of multiple analytes. However, a wearable system that utilizes arrays of many electrochemical sensors requires design of new microelectronic instrumentation that simultaneously meets demanding power, area, sensitivity (minimum linear response), noise and dynamic range performance goals. In particular, each target gas is present in a different range of possible concentrations: toxic gases can be harmful at concentrations as low as parts per billion (ppb) while some atmospheric gases of interest, such as O_2, are present in concentrations ten million times larger. As a result, a sensor array can generate a wide range of DC current outputs, and thus the instrumentation electronics should be able to measure currents at sub-pA level (to achieve high sensitivity for scarce target gases), at the μA level (for large concentration atmospheric gases) and all ranges in between [10]. Therefore, power-efficient, compact, amperometric instrumentation with wide dynamic range and a sub-pA limit of detection is desired.

The literature contains numerous examples of CMOS amperometry instruments paired with customized analog-to-digital converters (ADCs). Current-mode incremental ΣΔ ADCs achieve sub-pA sensitivity [11, 12], but power consumption increases rapidly for larger input currents because the reference current needs to be larger than the input current. Integration and current-to-frequency (I-to-F) ADC based designs can only achieve tens of pA sensitivity [13–15]. Voltage-mode SAR ADCs [16, 17] show good performance but cannot achieve the sensitivity of incremental ΣΔ ADCs. To expand the input current range, a scale-down method using current mirrors [15], or a hybrid ADC (I-to-F plus integration ADC) topology was used [18], but these circuits are not power and area efficient and can only achieve tens of pA sensitivity. A circuit combining incremental ΣΔ ADC and SAR ADC was shown to extend range but consumes huge (38 mW) power [19]. In summary, none of these circuits can simultaneously provide tight area, power (micro watt level), sensitivity (sub-pA level) and dynamic range constraints imposed by wearable amperometric gas sensor arrays for measurement of multiple targets in wide ranges. This paper details the design of a power-efficient high-performance amperometric ADC capable of resolving sensor responses for a broad range of target concentrations. The circuit employs a novel input current modulation approach and a ΣΔ ADC to achieve 164 dB cross-scale dynamic range and a detection limit of 100fA at only 241 μW per channel, a combined performance that has not been achieved by existing work. This paper expands on preliminary results [10] by reporting comprehensive analysis of performance limitations, presenting complete circuit characterization, and showing new results from electrochemical experiments. Section II analyzes existing solutions for amperometric sensor circuits and introduces the input modulation concept as a solution to the power vs. dynamic range tradeoff. Sections III and IV describe the design and implementation of the input modulated ΣΔ ADC. In section V, expressions for the transfer function and power efficiency of the circuit are derived, and the

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circuit performance limitations factors are analyzed. In section VI, circuit characterization and electrochemical experiment results are presented.

II. Approach and Circuit Concept

A. Gas Sensor Array Concept

Room temperature ionic liquid (RTIL) electrochemical sensors provide the sensitivity and selectivity of electrochemical sensing while overcoming the challenges of traditional electrolytes such as limited lifetime [20]. RTIL electrochemical sensors have demonstrated amperometric response to atmospheric gases like O_2 and CO_2 that are indicators of indoor air quality affecting human metabolism, and toxic pollutants such as NO_2, NO, CO, SO_2, H_2S [3, 21–25]. Our group is developing an RTIL sensor array to simultaneously measure the concentrations of multiple gaseous analytes. Fig. 1 shows the amperometric response of a single sensor to CO, SO_2, O_2 and H_2. Responses to other gases such as CH_4 and NO_2 have also demonstrated by our RTIL sensors [26, 27]. Arrays of such sensors can be employed to monitor gas mixtures using advanced signal processing algorithms [6, 28].

To implement miniaturized arrays of RTIL electrochemical sensors, we have developed a rapid-response structure on a porous Teflon substrate wherein each sensor element has an individual electrode and an individual electrolyte [3, 26]. This allows a variety of electrode materials and electrolyte chemical compositions to be used improve the sensor arrays ability to monitor a mixed-gas environment. Furthermore, because the sensor elements are physically isolated, this structure eliminates electrochemical crosstalk between sensor elements.

Implementing miniaturized electrochemical sensor arrays within a wearable system sets stringent requirements on the instrumentation circuitry. Because most applications desire sensors with the best detection limits possible, noise and circuit sensitivity are critical and ideally addressed by assigning a readout channel to each sensor element to avoid low-level-analog multiplexing. To convert readout channel results to digital signals for delivery off sensor, a circuit array architecture with a single time-multiplexed ADC could be used. However, this architecture requires multiplexing in the analog domain that contributes to crosstalk noise [29]. To eliminate electrical crosstalk, a pixel-level ADC architecture can be used in which an ADC is implemented for each sensor element and multiplexing is moved to the digital domain [30]. It has been shown that pixel-level ADC conversion can achieve better signal-to-noise ratio (SNR) and lower power consumption because conversion is performed physically close to the signal source and in parallel at low clock speeds [31]. Because these characteristics are well suited to the performance requirements of wearable amperometric sensor arrays systems, we chose the pixel-level ADC architecture to implement our multi-channel electrochemical array readout.

The pixel-level ADC should be compact and low-power to improve the system's portability and longevity, and the impact of this requirement is amplified when developing high-density sensor arrays. A miniaturized amperometric sensor array with small electrodes and a ppb-level detection limit requires instrumentation with sub-pA sensitivity. Elements in a gas sensor array can generate current levels ranging from sub-pA to several tens of μA

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depending on the target concentration range. Such a wide current span requires the readout circuit to have a large dynamic range.

B. Analysis of ADC Structures

Current mode incremental first-order ΣΔ structures tend to have the best sensitivity (fA range) of any class of ADC while remaining compact and consuming as little as a few μW of power [11, 12]. This ADC structure combines the benefits of integration and noise shaping of ΣΔ ADCs and achieves superior performance for instrumentation and measurement applications, namely high absolute accuracy and excellent linearity with small area and power costs [32]. Although such ADCs are not fast, environmental conditions do not change rapidly for most applications, making lower-bandwidth circuits attractive. Furthermore, the current mode, low power and high noise performance of this ADC structure allow this ADC to be used as pixel-level ADC. In contrast, SAR ADCs are not good as pixel-level ADC and mostly used as single time-multiplexed ADCs [16, 17] because of two reasons: (1) the voltage mode of SAR ADCs requires a current-to-voltage (I/V) convertor; (2) the lower noise performance of SAR ADC requires an addition gain stage. Both I/V convertor and gain stage consume additional power and area. Finally, incremental ΣΔ ADCs are structurally compatible with digital modulation technique in this work as described below. Therefore, this work uses the current-mode incremental ΣΔ ADC to build pixel-level ADCs.

Unfortunately, traditional ΣΔ ADCs require reference current supplies larger than their input (measured) current, which dominates the system's power budget when input magnitudes exceed a few μA [10]. Another limitation of conventional current-mode ΣΔ ADCs is that, to accommodate a large input range, a multiple-bit current-mode digital-to-analog converter (DAC) is needed as a reference. This reference current DAC can occupy a large chip area and have high power consumption, limiting the number of readout channels. These limitations motivated our design of a circuit block for prescaling the input current by a programmable attenuation factor, improving power efficiency for larger input currents. This scaling factor provides the user with a means to select a current range appropriate to the sensing target. To conserve chip area, an ADC design using this technique can share the same reference current generator between multiple input current ranges.

C. Current Scaling Approaches and Circuit Concept

A digital modulation scheme was chosen for prescaling the input current. An alternative analog method employing current mirrors is feasible, but it suffers power and precision problems due to device mismatch and occupies large area to achieve large scaling ratio [12]. In contrast, digital modulation can be simply implemented by a single compact CMOS switch, allowing for precise control of device ratios, low area overhead, and low power. A digital modulation circuit is also much easier to reconfigure at runtime.

By modulating the input current I_{in} with a square wave having a precisely controlled duty cycle of $1/M$, the average current seen by the ADC input can be reduced to I_{in}/M. This reduces the ΣΔ ADC reference current requirement by a factor of M. The input current range can be reprogrammed by changing the duty cycle of the modulating pulse train. Fig. 2 illustrates this digitally modulated input current concept.

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III. Circuit Block Design

A. ΣΔ ADC design

To demonstrate the proposed input modulation ΣΔ ADC architecture, a current-mode ΣΔ ADC block is needed. A semi-synchronous incremental ΣΔ design was chosen as the starting point of this ΣΔ ADC block because it has been demonstrated to be very compact and achieve fA sensitivity with only μW power per channel [11]. Fig. 3(a) shows the block-level schematic for the base ADC design. The circuit uses an integrator and a hysteretic comparator to produce two 1-bit pulse-width-modulation (PWM) digital pulses, D and D*, that modulate two reference currents, I_{refP} and I_{refN}. I_{refP} and I_{refN} inherently suffer from mismatch, requiring post-fabrication calibration and reducing measurement resolution [30]. However, notice that amperometric sensors typically measure current in only one direction, depending on whether oxidation or reduction of the target compound(s) is being recorded. Thus, only one reference current is necessary to complete the negative feedback path required by the ΣΔ algorithm. This feature allows only one reference current to be employed, resolving the mismatch issue. In addition, an improvement in noise performance is expected because only one reference current source contributes to noise. The resulting simplified ΣΔ ADC schematic shown in Fig. 3(b) contains only a reference current sink I_{ref}. This circuit measures a sensor cell with current flowing out of the sensor. For cells with the opposite current direction, a single current source I_{ref} controlled by the ΣΔ modulator output D can be used for measurement.

To simplify analysis of the circuit's behavior, assume that the comparator in Fig. 3(b) has no hysteresis. The new incremental ΣΔ ADC is then governed by the transfer function

$$\overline{I'_{in}} = \frac{\int_0^{T_t} I'_{in}(t)\,dt}{T_t} = \frac{I_{ref} T_s \sum_{i=1}^{N} D_i^*}{T_t} = \frac{I_{ref} \sum_{i=1}^{N} D_i^*}{N} \quad (1)$$

where I'_{in} is the input current of the ΣΔ ADC, $\overline{I'_{in}}$ is the average value of I'_{in} over the integration time T_t, t is time, T_s is the sampling clock period and equal to $1/f_s$, D_i^* is the value of D* at time index i, and N is the total number of pulses in a conversion cycle of the ADC and equal to T_t/T_s.

B. Input modulation stage design

A switch controlled by the modulation signal was chosen to implement the input modulation stage because it is compact and consumes almost no static power. As shown in Fig. 2, the input DC current is modulated by a square wave with a pulse width of T_p and a period of T_m. The modulated current can be expressed as a Fourier series as

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$$\begin{cases} I'_{in}(t)=I_{in}\sum_{k=-\infty}^{\infty}a_k e^{jk\omega_m t}, k=0,1,2,\cdots \\ a_k=\frac{\sin\frac{k\omega_m T_p}{2}}{k\pi}, k\neq 0 \\ a_0=\frac{T_p}{T_m}=\frac{1}{M} \end{cases} \quad (2)$$

where ω_m is the modulation signal's angular frequency and is equal to $2\pi/T_m$.

From (1) and (2), $\overline{I'_{in}}$ can be represented as

$$\overline{I'_{in}}=\frac{\int_0^{T_t} I'_{in}(t)\,dt}{T_t}=\frac{I_{in}}{M}+I_{in}\sum_{k=-\infty}^{\infty}\frac{(\int_0^{T_t} a_k e^{jk\omega} m^t dt)}{T_t} \quad (3)$$

On the right side of (3), the first term is the desired one and shows that input I_{in} is prescaled by a factor of $1/M$; the second term is undesired and represents harmonic distortion due to modulation. To zero the second term, T_t needs to be an integer multiple of T_m. To simplify the implementation of the clocking circuit, T_p was set equal to T_s, the ADC's sampling period. As a result, $T_m = MT_s$, and $T_t = LMT_s = NT_s$. where L, M, N are integers. The resulting modulation signal is shown in Fig. 4.

C. Current buffer and biasing potentiostat design

A chronoamperometric sensor can be a two-electrode system or three-electrode system. In both systems, sensor output current can be measured from the sensor's working electrode (WE), which must be held at a constant bias to stabilize the output current. The output settling time can be as much as several hours after a new potential is applied [26, 33], necessitating a current buffer to maintain a constant electrode bias when the modulation switch disconnects the sensor from the circuit input. A current conveyor is a small, very low-power choice of current buffer circuit [34]. A current conveyor illustrated with a two-electrode system in Fig. 5(a) was used. Here the WE voltage is controlled by V_{WE}. A current mirror is used in the current conveyor to isolate WE from the input modulation stage. OTA2's transistors are operated in the sub-threshold region, yielding sub-μA current consumption. As a result, the power efficiency of the circuit is good for large input currents. When the input current is small compared to the current consumed by the current conveyor, the current conveyor and input modulator may be disabled to save power, leaving only the simplified ΣΔ ADC.

A three-electrode electrochemical sensor contains an additional counter electrode (CE). These sensors require an additional biasing potentiostat to control the potential difference V_{cell} between the working and reference electrodes and to provide current to the CE [35, 36]. Because WE voltage is controlled by V_{WE} in Fig. 5(a), only RE voltage needs to be controlled. Voltage followers are widely used as for such a purpose, especially for electrochemical sensor array applications [13, 35]. The schematic of a voltage follower in a three-electrode system is shown as opamp1 in Fig. 5(b). The biasing potentiostat opamp1

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holds the RE voltage at $V_{RE.}$ WE voltage is set by the current readout circuit, as it is in Fig. 5(a).

D. Full input modulated ΣΔ ADC design

Combining all the design choices discussed above, a block diagram of the complete input modulated ΣΔ ADC is shown in Fig. 6. The readout channel consists of a current conveyor, modulation, and simplified ΣΔ ADC stages. An additional/optional biasing potentiostat for three-electrode sensors is also shown. A capacitor array C_f was chosen as the integrator feedback capacitance to provide programmable integration gain. This circuit can readout electrochemical sensors in which current flows unidirectionally out of the working electrode. For sensors that draw current into the WE, a current conveyor with an NMOS current mirror may be used instead, or a bidirectional current conveyor [37] could be used for sensors that need to measure both oxidation and reduction reactions.

IV. Transistor Level Circuit Implementation

A. Sub-circuits of ΣΔ modulator

OTA1 in the integrator in Fig. 6 was implemented as a folded-cascode amplifier, as shown in Fig. 7(a), because it achieves a good tradeoff between noise, output range, chip area, and power performance. PMOS input transistors with large area were used to reduce the flicker noise. The 1pF capacitor C_c was used to improve the circuit stability. M_{p7} and M_{p8} comprise the output stage, providing large current drive capability. A class AB output stage may be used to replace these two transistors for better power efficiency. The voltage V_{BIAS} sets the output stage bias current. For small input currents, the output stage can be disabled to maximize power efficiency by setting V_{BIAS} to V_{dd} and setting the multiplexer to bypass this stage. The current drive capability of the OTA1 was set to cover sensor outputs up to 10 μA to meet application goals.

A hysteretic comparator is needed by the semi-synchronous ΣΔ ADC to reduce the substrate noise interference and improve converter linearity [11]. A schematic of the comparator is shown in Fig. 7(b). The comparator consists of preamplification (preamp) and decision stages. The preamp stage enhances the comparator's sensitivity by providing a large gain and isolating the input from switching noise in the decision stage [38]. The decision stage is a positive feedback circuit, generating hysteretic output. The two hysteresis levels can be programmed by V_{biasP} and V_{biasN}. These two voltages also control the comparator's dynamic power by setting the switching current of a current starved inverter formed by M_{n3}, M_{n4}, M_{p4} and M_{p5}.

A counter is needed to act as a low-pass and decimation filter in an incremental ΣΔ ADC. This counter needs to be highly compact and power efficient for a wearable sensor array. To reduce area cost, the counter output needs to be serially transferred off-chip to simplify system-level interconnects. To implement this counter, an area and power-efficient counter/shifter design [30] was chosen that saves area by sharing the counter hardware with the serialization shifter and saves power by using current starved inverters.

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The reference current source I_{ref} in Fig. 6 needs to have low power, area, and noise. The schematic for the implemented current generator is shown in Fig. 8. M_{n1} and M_{n2} form a cascoded stage to generate a precise reference current. V_{b1} controls the value of I_{ref} and is generated by a low-power current splitting circuit [39]. This current splitting circuit can generate pA range currents while maintaining very low area because it does not require any capacitors or resistors [40]. The integrator input is virtually connected to analog ground by OTA1 in Fig. 6. To increase the switching speed and reduce switching noise, M_{n4} was used to set M_{n2}'s drain at analog ground when M_{n3} is turned off. To permit tuning of input current range of other performance parameters, I_{ref} was implemented as a programmable current array with a maximum value of 500 nA.

B. Input modulation stage, and current conveyor

The input modulation stage is simply a CMOS switch and is therefore very small and low power. Switching noise is minimized by using a transmission gate structure, minimum size transistors and dummy transistors. Although the on-resistance of this switch can form a low-pass filter with the current conveyor's output capacitance [41, 42], the sensor output frequency is very low (almost DC) and this filter has negligible effect on the input signal.

In the current conveyor in Fig. 6, OTA2's output is connected to the gate of transistor M_f. Therefore, no output stage is needed, and OTA2 can be very low power and compact. OTA2 used the same design as OTA1 in Fig. 7(a), without the output stage. The current mirror was implemented with a cascoded structure to improve accuracy, and the mirror ratio was set at 1 to maximize accuracy and minimize the area. To set the output node voltage to analog ground when the input modulation stage is turned off, a transistor like M_{n4} in Fig. 8 was included in the current mirror design.

V. Theoretical Analysis

A. Transfer function

The modulated input current at the ADC stage I_{in}' in Fig. 6 can be expressed as

$$I_{in}'(t)=\begin{cases} I_{in}, & n\cdot M\cdot T_s \le t < n\cdot M\cdot T_s+T_s \\ 0, & else \end{cases} \quad (4)$$

where $n = 0, 1, 2, \ldots L\text{-}1$; T_s is the sampling clock period, and M is the modulation factor as in Fig. 4.

Substituting (4) into (1), the transfer function of the input modulated ΣΔ ADC is given by

$$I_{in}=\frac{I_{ref}}{L}\sum_{i=1}^{N} D_i^* \quad (5)$$

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where L is the total number of '1' pulses in the modulation waveform, as defined by Fig. 4. Because (5) is independent of the sampling clock cycle T_s and the integrator feedback capacitance C_f, no precise clock or capacitor components are needed to operate the input modulated ΣΔ ADC.

B. Power analysis

If we define α as the average duty cycle of D^* such that $0 \leq \alpha \leq 1$, then (for a constant input) the summation in (5) becomes

$$\sum_{i=1}^{N} D_i^* = \alpha N \leq N \quad (6)$$

Since $N = L \times M$, substituting (6) to (5), yields

$$I_{in} = \frac{I_{ref}}{L}\alpha N = I_{ref} \times \alpha M \leq I_{ref} \times M \xrightarrow{thus} I_{ref} = \frac{I_{in}}{\alpha M} \geq \frac{I_{in}}{M} \quad (7)$$

When $\alpha = 1$, $I_{ref} = I_{in}/M$; setting $M = 1$ produces the I_{in} to I_{ref} relationship of an unmodulated ΣΔ ADC. Thus (7) shows that the input modulated ΣΔ ADC scales down the required magnitude of the reference current I_{ref} by a factor of M for a given I_{in}. This also shows that the input modulated ADC can expand maximum input current by a factor of M; in other words it can improve the input current range by $20\log_{10}(M)$ dB.

To evaluate power improvement, the power consumption of the input modulated ADC was compared to that of an unmodulated ADC. Both versions use the same unmodulated simplified semi-synchronous ΣΔ ADC core as in Fig. 3(b), with the same integrator, comparator, D flip-flop and counter, but with different reference current values. The modulated version adds input modulation and current conveyor stages. Since the biasing potentiostat stage would be the same for both versions, it was omitted from this analysis. Because the digital components in both versions are largely the same and their power consumption will change negligibly with sensor input current, we can assume that, excluding the reference current I_{ref}, both versions consume the same ΣΔ ADC core current I_a. If the input current I_{in} is DC, then the unmodulated ADC reference current I_{ref_um} must obey $I_{ref_um} \geq I_{in}$ from (7). The minimum power P_{um} of the unmodulated ADC is therefore

$$P_{um} = [\,min\,(I_{ref_um}) + I_a]V_{dd} = (I_{in} + I_a)V_{dd} \quad (8)$$

which shows that P_{um} directly increases with I_{in} when $I_{in} \gg I_a$. (7) gives $\alpha\, I_{ref_m} \geq I_{in}/M$. Similarly, the minimum power P_m of the modulated ADC is given by

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$$P_m=[min\ (I_{ref_m})+\overline{I'_{in}}+I_a+I_{cc}]V_{dd} \xrightarrow{\overline{I'_{in}}=\frac{I_{in}}{M}} P_m=[2I_{in}/M+I_a+I_{cc}]V_{dd} \quad (9)$$

where I_{cc} is the current dissipated by the current conveyor, $\overline{I'_{in}}$ is the average current flowing through the input modulation stage, and I_{ref_m} is the unmodulated ADC reference current. The simplified form of (9) is obtained by noticing that (3) gives $\overline{I'_{in}}=I_{in}/M$ and (7) gives min(I_{ref_m}) = I_{in}/M.

Defining a power improvement factor as η_Δ = (P_{um}-P_m), we have

$$\eta_\Delta=(P_{um}-P_m)=[(1-\tfrac{2}{M})I_{in}-I_{cc}] \quad (10)$$

When input currents are small, M=1 and η_Δ is negative indicating the modulated version requires more power. However, the difference is small in value because I_{in} is small. Furthermore, when M=1 the current conveyor and input modulator can be powered off to reduce power consumption. On the other hand, when I_{in} is large enough that M > 2 and I_{in} > I_{cc}, then η_Δ is positive and the modulated version starts to save power. For example, if M=32 and I_{cc} =1μA (which is readily achievable by operating OTA2's input transistors in the subthreshold region), then $\eta_\Delta > 0$ for any $I_{in} \geq 1.07$ μA. As I_{in} gets larger, M is increased and the input modulated ADC can achieve significantly lower power consumption than the unmodulated ADC.

C. Input modulation effect on resolution, and signal range

This section analyzes the effect of input modulation on the ADC performance. The ideal least significant bit (LSB) resolution of the input current I_{inLSB} can be estimated by substituting $\sum_{i=1}^{N} D_i^*=1$ into (5), and the maximum input current I_{inMAX} can be estimated by substituting $\sum_{i=1}^{N} D_i^*=N$ into (5). These substitutions yield

$$\begin{cases} I_{inLSB} & =\frac{1}{L}I_{ref} \\ I_{inMAX} & =MI_{ref} \end{cases} \quad (11)$$

where L, M, and N are defined in Fig. 4. For a fixed I_{ref}, larger L corresponds to a smaller LSB value and the maximum input current is proportional to the modulation factor M. In practice these ideal parameters are limited by circuit constraints. I_{inMAX} is limited by the drive current ability of OTA1 in Fig. 6. I_{inLSB} is limited by noise effects discussed below.

Output saturation in the ΣΔ ADC's integrator can cause large errors. Therefore, it is important to calculate the integrator output swing. The largest integrator output swing

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happens when the input current is equal to I_{inMAX} in (11) and the input modulation stage is on. Defining the hysteresis level as Δ, the maximum output swing, V_{range}, is

$$|V_{range}| \leq \Delta + \frac{I_{inMAX} T_s}{c_f} = \Delta + \frac{M I_{ref} T_s}{c_f} \quad (12)$$

where C_f is the integrator's feedback capacitance, T_s is the modulation signal pulse width. (12) shows that the integrator's output range can limit the maximum input current. To mitigate this effect, large C_f and small T_s were used to reduce the integrator output swing for large input current.

D. Noise analysis and performance limitations

The finite gain of OTA1 in the integrator weakens the ADC's noise shaping performance in a similar manner to the traditional incremental ΣΔ ADC [43]. This section studies other major noise sources associated with the input modulated ΣΔ ADC.

1) Current conveyor—The current conveyor is one of the major contributors to the input referred noise of the ADC because it is the first stage of the circuit. Mismatch in the current conveyor would increase output linearity error and reduce the overall sensitivity. Fig. 9 shows the current conveyor schematic with a cascoded current mirror to reduce current mismatch [44]. The current conveyor's noise model in Fig. 9 shows the transconductance and dimension of M_{p1} and M_{p2} are equal. A similar structure for OTA2 and M_f has been reported [18]. The loop gain formed by OTA2 and M_f greatly reduces M_f's contribution to the input referred current noise [18]. Adding noise from M_{p1} and M_{p2}, the input referred current noise of the current conveyor is

$$i_{ineq}{}^2 = (2\pi f)^2 C_{in}^2 e_n^2 + \frac{16kT\, g_{m_p}}{3} + \frac{2K_{fp} g_{m_p}{}^2}{C_{ox} W_p L_p f} \quad (13)$$

where the second and third terms are the thermal noise and flicker noise of M_{p1} and M_{p2}, f is the frequency, k is the Boltzmann constant, T is the operating temperature in Kelvin, g_{m_p} is the transconductance of M_{p1} and M_{p2}, K_{fp} is a process-dependent constant, and C_{ox} is the gate oxide capacitance per unit area. g_{m_p} can be expressed as $\sqrt{2\mu_p C_{ox} I_{in} W_p / L_p}$, where μ_p is the hole mobility. Substituting g_{m_p}'s expression into (13) yields

$$i_{ineq}{}^2 = (2\pi f)^2 C_{in}^2 e_n^2 + \frac{16kT\sqrt{\mu_p C_{ox} I_{in} W_p / L_p}}{3} + \frac{4K_{fp}\mu_p I_{in}}{L_p^2 f} \quad (14)$$

Therefore, to reduce the input referred current noise contribution from the conveyor, e_n, W_p/L_p was set to be small and L_p was set to be large. Small C_{in} can be achieved by reducing

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biosensor capacitance and parasitic capacitance. Monolithic integration can effectively reduce C_{in} by decreasing the parasitic capacitance [45].

2) Input modulation stage—The noise analysis of the input modulation stage can be simplified by modeling the modulator as an NMOS switch SW, as shown in Fig. 9. The modulation switch contributes to both static and dynamic noise. The static noise refers to the noise components I_{n3}^2 generated by the turn-on resistance of the switch [41, 42, 46]. Because transistor SW forms a cascode with device M_{p2} when it is on, its static noise contribution is negligible. The dynamic noise refers to the error caused by charge injection and clock feedthrough. Small transistors were used to reduce this noise source. A complementary structure with dummy transistors was also used to further reduce the charge injection noise.

Jitter in the modulation signal can cause output errors. Assuming the average pulse width of the modulation signal is T_s, and the pulse jitter for the jth pulse is ΔT_s(j) yields

$$I_{in} \cdot (L \cdot T_s + \sum_{j=1}^{L} \Delta T_s(j)) = I_{ref} T_s \sum_{i=1}^{N} D_i^* \quad (15)$$

The second term on the left of (15) represents the error due to clock jitter. If ΔT_s(j) follows a Gaussian distribution, this clock jitter noise is rejected by the summation operation (to a first order). Large L, i.e. sampling for a longer time, was thus used to provide better jitter noise rejection.

3) ΣΔ Modulator—OTA1's finite gain, slew rate, and bandwidth limit the input modulated ΣΔ ADC's performance in the same way they do with a conventional ΣΔ ADC. The finite gain of OTA1 causes integrator leakage and weakens the noise shaping performance [43]. The slew rate and bandwidth limit the integrator's settling time and increase the output error [43].

The noise model of the integrator in the input modulated ADC is shown in Fig. 10. The input referred noise of OTA1 is $e_{n_int}^2$, and the total admittance at the integrator's input node is Y_M. Y_M includes the admittance looking into the input modulation stage and parasitic capacitance at OTA's negative input terminal. Referring to the noise analysis of the integrator in [47] and using the total integration time $T_t = LMT_s$, the input referred current noise of OTA1 during integration is derived as

$$\begin{aligned} I_{ni_int}^2 &= e_{n_int}^2 \left(\frac{Y_M}{T_t s} (1 - e^{-T_t s}) \right)^2 M \\ &= e_{n_int}^2 \left(\frac{Y_M}{\sqrt{M} \cdot L T_s s} (1 - e^{-T_t s}) \right)^2 \end{aligned} \quad (16)$$

where $e_{n_int}^2$ is OTA1's voltage noise; s is the Laplace variable, and T_t is the total integration time in one ADC conversion cycle. The factor of M is due to the input

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modulation. Although operating the OTA1's input transistors M_{p1} and M_{p2} in subthreshold region increases $e_{n_int}^2$,, these transistors were set at large area to reject flicker noise and reduce their noise impact. Furthermore, gas sensing applications allow setting a long integration time T_t (~1s), to reduce the overall noise $I_{ni_int}^2$.

When the input modulation stage is on, the impedance looking into the input modulation stage is a very large resistance, formed by the cascoded transistors M_{p2} and M_{p4}, in parallel with the very small drain capacitance of transistor SW. When the input modulation stage is off, this impedance is very large because the modulation switch is off. In either case, the impedance looking into the modulation stage is very large, and the admittance Y_M is very small. On the other hand, an incremental ΣΔ ADC generally uses very large T_t to achieve a very high resolution, meaning that L and M are large. As a result, the equivalent input referred current noise of OTA2 is negligible.

The reference current noise is dominated by M_{n1} in Fig. 8. This noise is modulated by the 1-bit output D* of the ΣΔ modulator, which can be modeled by a multiplicative factor of $\sum_{i=1}^{N} D_i^*/N$. The equivalent input referred current noise of the reference current is

$$I_{ni_ref}{}^2 = \left(\frac{8kT\, g_{m_n}}{3} + \frac{K_{fn} g_{m_n}{}^2}{C_{ox} W_n L_n f}\right) \times \frac{\sum_{i=1}^{N} D_i^*}{N} M \quad (17)$$

where g_{m_n} is the transconductance of M_{n1} in Fig. 8, W_n and L_n are M_{n1}'s size, and K_{fn} is the NMOS flicker noise constant. g_{m_n} can be expressed as $\sqrt{2\mu_n C_{ox} I_{ref} W_n / L_n}$, where μ_n is the electron mobility Substituting g_{m_n}'s expression and (5) into (17) yields

$$I_{ni_ref}{}^2 = \left(\frac{8kT\sqrt{2\mu_n C_{ox} \frac{W_n}{L_n}}}{3\sqrt{I_{ref}}} + \frac{2K_{fn}\mu_n}{Ln^2 f}\right) I_{in} \quad (18)$$

To reduce the reference current contribution to input referred current noise, W_n/L_n was set to be small, and L_n was set to be large. To reduce the charge injection noise due to modulation of I_{ref} (via D and D^*), very small area was used for M_{n3} and M_{n4} in Fig. 8.

VI. Experimental Results

The input modulated ΣΔ ADC was fabricated in 0.5 μm CMOS, and the chip photograph is shown in Fig. 11. Eight recording channels were built on a 3×3 mm^2 chip. The biasing potentiostat was added for testing three-electrode sensors, and the output buffers are only needed for chip testing purposes. Omitting these elements, the active area of the readout circuit is 0.157mm^2, allowing integration of over 50 readout channels on a 3×3 mm^2 chip area. To produce control clocks and acquire the ADC output results, a digital hardware block was implemented in a Spartan 3E FPGA. A Faraday cage was used during testing to

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suppress 60-Hz line and other environmental noise. The whole chip was powered by a low-noise 5V supply.

A. Electrical Characterization

To characterize the circuit performance, a General Purpose Interface Bus (GPIB) controlled high resolution current source (model 6430 SourceMeter, Keithley Instruments) was used to generate input currents. For all measurements, the number of pulses in a conversion cycle, N as defined in Fig. 4, was set at 10^5. When the sampling frequency is 100 kHz, the ADC conversion time T_t is 1 s, which is an integer multiple of 60 Hz power-line frequency. As a result, the line frequency is suppressed by the counter's summation operation [32]. The hysteresis level of the comparator was set at 100mV. First, the input modulation was turned on by setting the modulation factor M at 8, 16 and 32 to study M's effect on current ranges. The reference current I_{ref} was set at 70nA and 500nA to study how the input current ranges are affected by I_{ref} at a fixed value of M. The normalized ADC output curves for different I_{ref} and M are shown in Fig. 12, which shows that larger M and I_{ref} shift the ADC response curve toward larger input current ranges.

Next, to test measurement of small currents, the input modulation was turned off by setting M to 1. The sampling frequency was kept at 100 kHz and N was kept at 10^5. Fig. 13 shows the ADC outputs for low input currents, normalized to the ADC output full range. Without input modulation, the ADC can measure currents from 3 nA to 493 nA. With a fixed I_{ref}, the modulation technique expands the ADC maximum input current to 16 μA, and thereby improves the input current range by 30 dB without significant power increase. If desired, the maximum input current could be further expanded by increasing the output current drive of OTA1 so that M can go beyond 32. Fig. 13 shows that a sensitivity (minimum linear response) as low as 100 fA can be achieved. As a result, the cross-scale dynamic range of the circuit is 164 dB.

Using the data from Fig. 12, the linearity and accuracy of circuit were quantified by the integral nonlinearity (INL) and differential nonlinearity (DNL) parameters, as shown in Fig. 14. Both parameters are defined in dB as errors divided by full range of the input current. When M is 32, the largest DNL is −46.8 dB and the largest INL is −40.52 dB, corresponding to 6.7 bit error. When M is 1, the largest DNL is −47.96 dB and the largest INL is −47.79 dB, corresponding to 8 bit error. The compensation steps used for the semi-synchronous ΣΔ ADC [11] can reduce the nonlinearity errors. Simulation reveals that the current conveyor's current mirror can limits the INL and DNL performance. The statistics of the largest INL and DNL for M = 4, 8, 16, 25, 32 indicate that the median INL and DNL are −46.0 dB and −40.0 dB, respectively; and the standard deviations of INL and DNL over all choices of M are 3.1dB and 2.1 dB. This shows that the INL and DNL do not depend substantially on the choice of M.

Table I illustrates the comparison between this work and other amperometric sensor instrumentation circuits. For a fair comparison, all the data is for electrochemical readout circuits. The biasing potentiostat's power consumption is omitted. Among the surveyed designs, this work achieves the largest dynamic range, the second best sensitivity and second best input range vs. power (RvP) factor. The RvP factor normalizes each circuit's power

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efficiency. Compared to the circuit with the best sensitivity [11], our circuit has 10× better RvP factor and 160× the current range, while the sensitivity difference is only 50 fA. Compared to the circuit with the best RvP factor [15], our circuit has 460× the sensitivity.

B. Electrochemical Experiments

To validate our circuit in sensor applications and highlight its ability to measure large input current using the input modulation method, electrochemical measurements were performed using a standard potassium ferricyanide ($K_4[Fe(CN)_6]$) solution. The solution was prepared by diluting $K_4[Fe(CN)_6]$ with a 0.1M KCL buffer. A three-electrode electrochemical system was built using electrodes from CH Instruments, Inc. The voltage between WE and RE was set at 0.39 V. The input modulation factor M was set at 32 and the reference current I_{ref} was set at 500 nA. The transient ADC responses for 15 mM, 20 mM, 25 mM and 30 mM $K_4[Fe(CN)_6]$ solutions were recorded and converted back to input current. The measurement results are shown in Fig. 15(a). The current output for the 30 mM solution reaches the full range of the ADC during the first several seconds, and then settles off to a plateau. The measured WE voltage remains stable because the current conveyor can support a much larger input current than the following ADC stage. The currents at steady-state electrochemical conditions (at $t = 200$ s) for different solution concentrations were extracted to plot the calibration curve in Fig. 15(b), which shows very good linearity, with an R^2 fit error of 0.995.

To validate the function of the circuit in a different current range with different modulation factor, the input modulated ADC with NMOS-current-mirror was used to read out an RTIL electrochemical sensor. The modulation factor M was set at 8. The voltage between WE and RE was set at −1.23 V to measure oxygen as an example gas. The oxygen concentrations were changed every 30 s. The oxygen concentration values and the transient ADC responses are shown in Fig. 16(a). The sensor output current is lower than that in Fig. 1(c) due to miniaturized electrode sizes. The corresponding calibration curve is shown in Fig. 16(b), and shows good linearity with a R^2 value of 0.9986.

VII. Conclusion

This paper reports an input current modulated ΣΔ ADC for portable amperometric sensor arrays. By modulating the input current before digitization with a semi-synchronous incremental ΣΔ ADC, large dynamic range is achieved with very good power efficiency and sub-pA sensitivity. Comprehensive analysis of performance limitations was applied to guide the circuit design. Fabricated in 0.5 μm CMOS, the circuit's compact size allows it to be scaled to over 50 readout channels on a 3×3 mm^2 chip. Compared to an unmodulated ΣΔ ADC, by setting the current modulation factor at 32, the measured input current range of the circuit can be improved by 30 dB without a significant increase in power and area. The input modulated ΣΔ ADC was measured to achieve 100 fA sensitivity and 164 dB cross-scale dynamic range with high power efficiency. Example electrochemical sensor experiments were conducted to validate the circuit's capability to measure different current ranges in real sensing applications. The combined performance of the current modulated ΣΔ ADC is well

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suited to applications of wearable/portable air quality monitoring for human health and safety.

Acknowledgments

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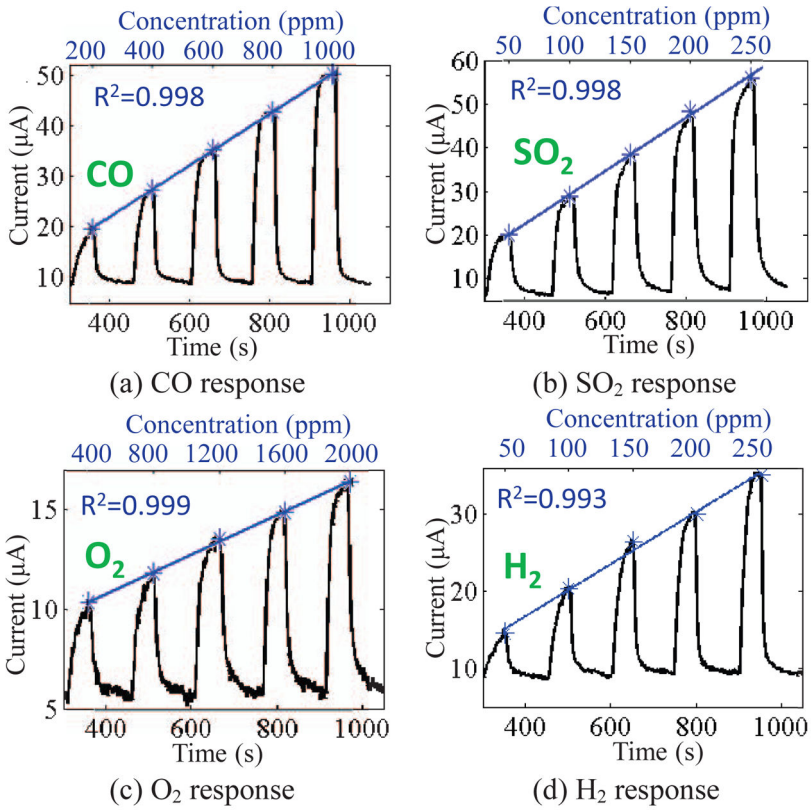

Fig. 1.

RTIL sensor responses for air quality monitoring. In the transient response of each gas, the five peaks represent five different concentrations. The valleys between peaks represent the sensor response when the concentrations were set at zero. The asterisks represent the stable sensor output currents at nonzero gas concentrations. The straight lines represent best-fitting lines.

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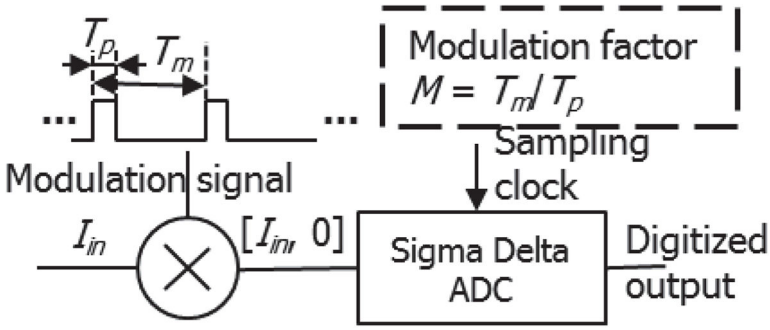

Fig. 2.

Concept of the input modulated ΣΔ ADC for portable amperometric gas sensor arrays. The modulation factor M is defined as the reciprocal of the modulation signal's duty cycle.

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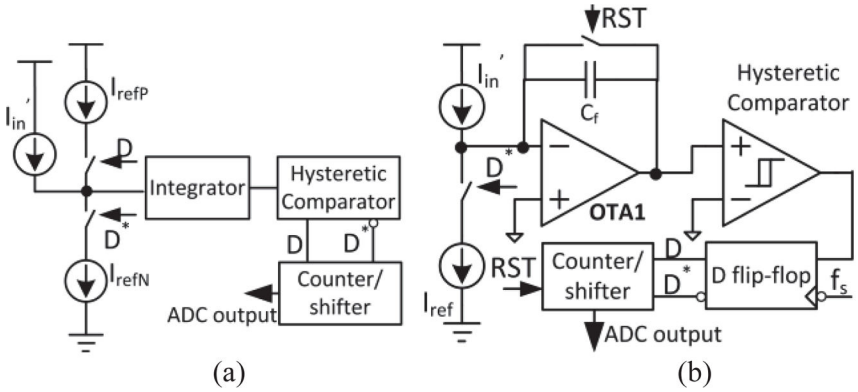

Fig. 3.

Schematic of (a) the semi-synchronous incremental ΣΔ ADC from [13] and (b) a simplified design for the target application. I_{in}' is the input current, f_s is sampling clock. D and D* are two inversed phase signals. I_{refP}, I_{refN} and I_{ref} are reference currents, modulated by D or D*. RST is a reset clock to reset the integrator and counter.

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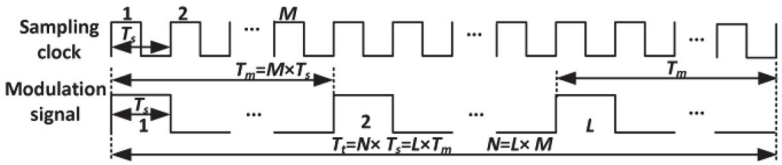
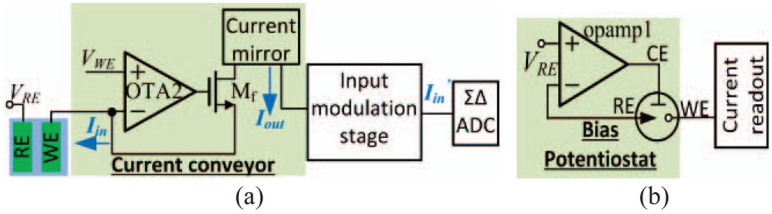


Fig. 4.

Control clocks for the input modulation stage and their relation to the ADC sampling clock. The conversion cycle of the incremental ΣΔ ADC is T_t. The modulation signal's cycle is T_m. L and M are integers.



(a) (b)

Fig. 5.

(a) Simplified schematic of the current readout circuit, including the current conveyor, and its connection to the input modulation stage and ΣΔ ADC. (b) Schematic of the biasing potentiostat circuit in a three-electrode system. I_{in} is the sensor output current, and I_{in}' is the modulated current. Reference electrode (RE), working electrode (WE) and counter electrode (CE) are the electrodes of the sensor.

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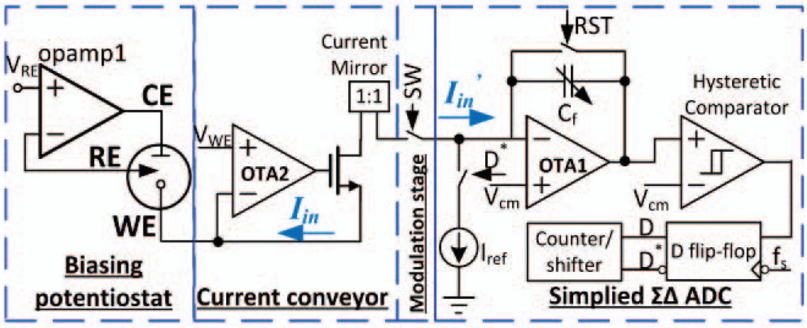

Fig. 6.

Simplified blocks of the input modulated ΣΔ ADC for three-electrode electrochemical sensors. Switch SW is controlled by the modulation signal in Fig. 3. f_s is the sampling frequency. I_{in} is the sensor output DC current and I_{in}' is the modulated current.

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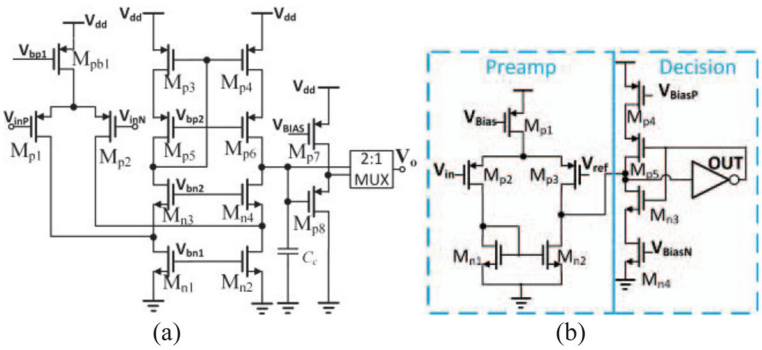

Fig. 7.

Schematic of the sub-circuits of the ΣΔ modulator: (a) the OTA used by theintegrator, and (b) the hysteretic comparator.

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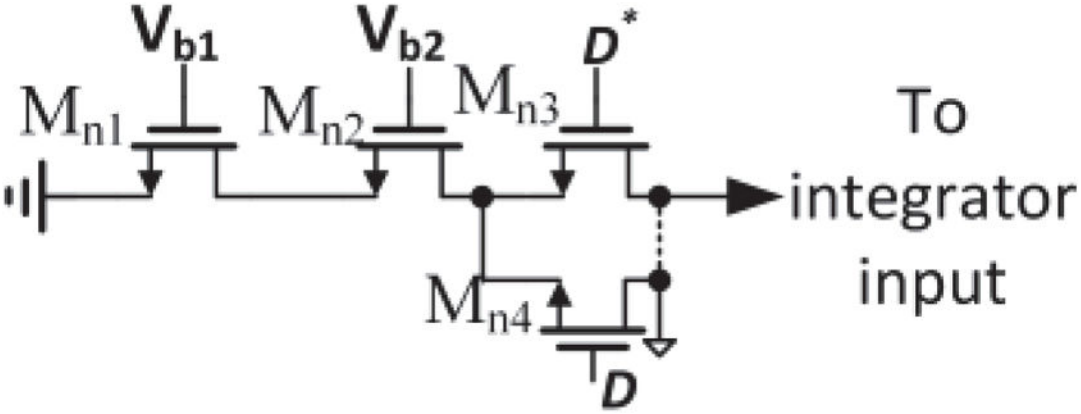

Fig. 8.
Schematic of the reference current generator I_{ref} in Fig. 6.

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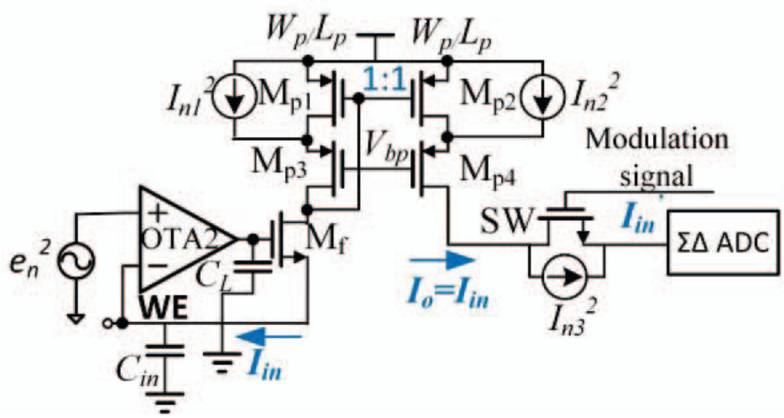

Fig. 9.

Noise model of the current conveyor and input modulation switch SW. C_{in} is the total capacitance at WE, including sensor capacitance, wiring capacitance and parasitic capacitance. e_n^2 is the OTA1's input referred voltage noise, I_{n1}^2 and I_{n2}^2 are the current noise of transistors of M_{p1} and M_{p2}, W_p and L_p are the dimension of transistor M_{p1} and M_{p2}.

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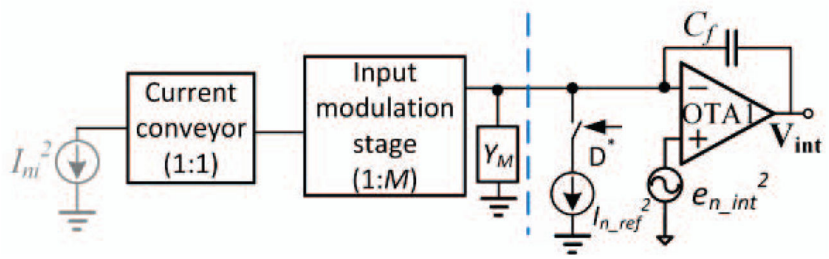

Fig. 10.
The noise model of the integrator and reference current.

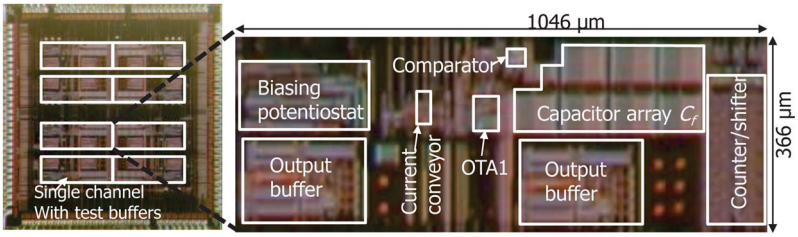

Fig. 11.

Chip photograph of the input modulated instrument.

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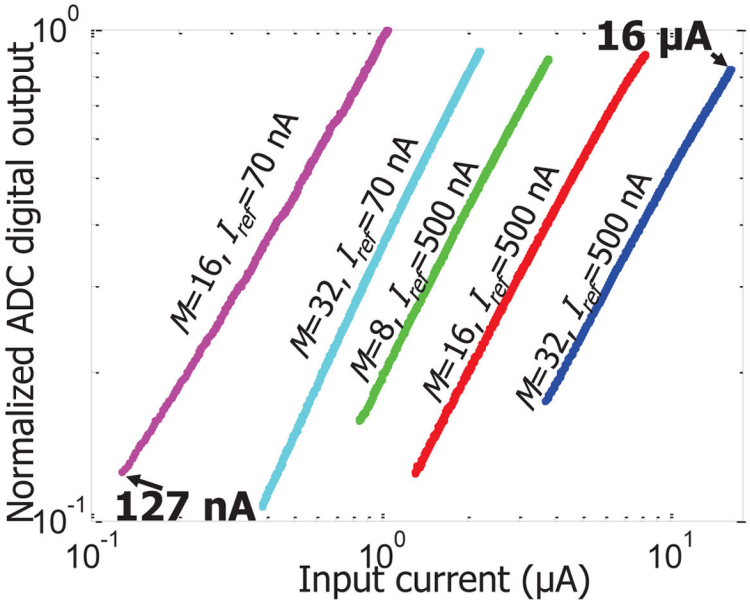

Fig. 12.

The normalized digitized output of the input modulation ΣΔ ADC for different input currents when input modulation is on. *M* is set at 8, 16, and 32.

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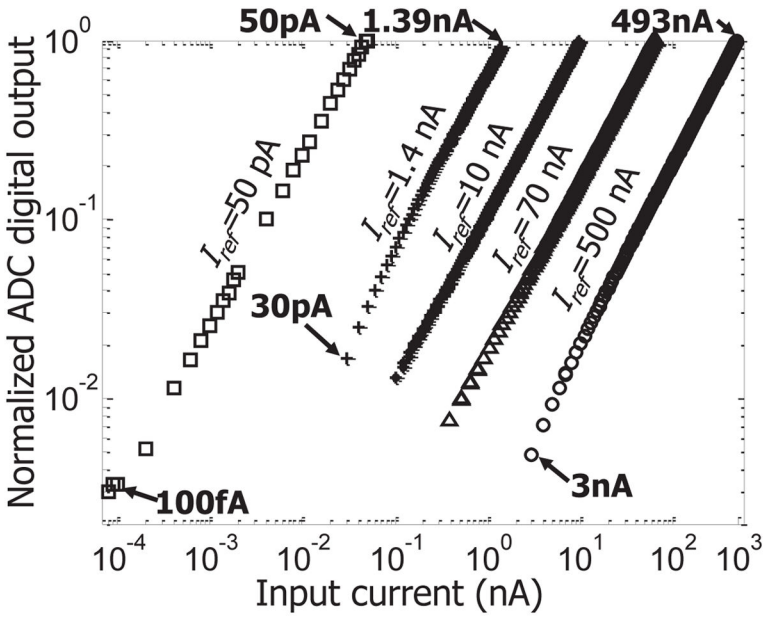
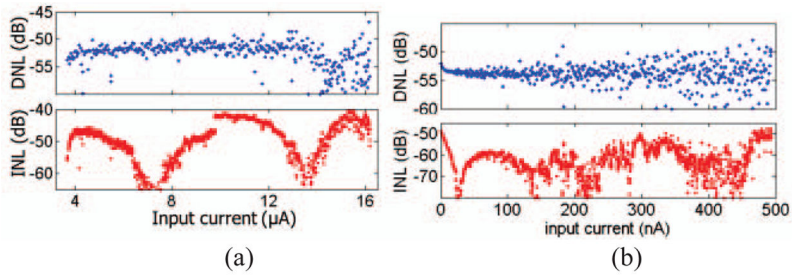


Fig. 13.

The normalized digitized output of the input modulation ΣΔ ADC for different input currents when input modulation is turned off by setting M at 1.



(a) (b)

Fig. 14.

Measured integral nonlinearity (INL) and differential nonlinearity (DNL) for (a) a modulation factor $M = 32$ and (b) $M = 1$. I_{ref} was set at 500nA for both measurements.

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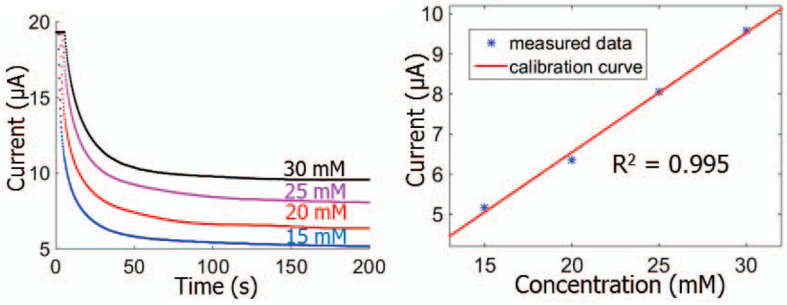

(a) (b)

Fig. 15.

Measured ADC response to a potassium ferricyanide ($K_4[Fe(CN)_6]$) solution. (a) ADC transient response, and (b) corresponding calibration curve.

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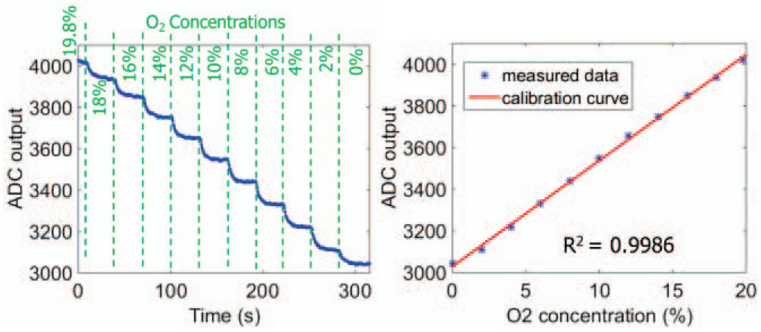

(a) (b)

Fig. 16.

Measured ADC response to ionic liquid O_2 sensor. (a) ADC transient response, and (b) corresponding calibration curve.

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TABLE I

Comparison between this Work and other Published Pixel-Level ADCs for Chronoamperomeric Sensor Arrays

	Max. Input Current	Sensitivity	Dynamic Range	Power/Chan.[3]	RvP[1]	Process	ADC structure
TCAS I '06 [11]	100 nA	50 fA	126 dB	11 μW	0.033	0.5 μm	Semi-synchronous sigma-delta
TBioCAS'07 [12]	0.5 μA	100 fA	140 dB	1300 μW	0.001	0.5 μm	Feedback modulated sigma-delta
TCAS I '06 [15]	50 μA	46 pA	120 dB	781 μW	0.578	1.2 μm	Integration
TBioCAS'13 [18]	350nA	24 pA	95 dB	188 μW	0.006	0.35 μm	Current to frequency + Single slope
This work	**16 μA**	**100 fA**	**164dB**	**241 μW**[2]	**0.331**	0.5 μm	Input modulated sigma-delta

[1] RvP (Input range vs. power) factor is defined as input current range (maximum value) divided by readout circuit's maximum consumed current.

[2] For fair comparison of other reported circuit without potentiostats, the biasing potentiostat's power consumption is omitted.

[3] Power/Chan. refers to power consumption per channel.