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IEEE Trans Biomed Eng. Author manuscript; available in PMC 2016 January 01.

Published in final edited form as:
IEEE Trans Biomed Eng. 2016 January ; 63(1): 120–130. doi:10.1109/TBME.2015.2406113.

Close-Packed Silicon Microelectrodes for Scalable Spatially Oversampled Neural Recording

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Abstract

Objective—Neural recording electrodes are important tools for understanding neural codes and brain dynamics. Neural electrodes that are close-packed, such as in tetrodes, enable spatial oversampling of neural activity, which facilitates data analysis. Here we present the design and implementation of close-packed silicon microelectrodes, to enable spatially oversampled recording of neural activity in a scalable fashion.

Methods—Our probes are fabricated in a hybrid lithography process, resulting in a dense array of recording sites connected to submicron dimension wiring.

Results—We demonstrate an implementation of a probe comprising 1000 electrode pads, each 9 × 9 μm, at a pitch of 11 μm. We introduce design automation and packaging methods that allow us to readily create a large variety of different designs.

Significance—Finally, we perform neural recordings with such probes in the live mammalian brain that illustrate the spatial oversampling potential of closely packed electrode sites.

Index Terms

Extracellular; Microelectrodes; Neural Recording; Spatial Oversampling; Electrode Array; Silicon Probe

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I. Introduction

The need for close-packed neural recording electrodes arises from the desire to record the activity of a single neuron from multiple points in space, which facilitates the data analysis [1],[2]. Stereotrodes and tetrodes, which contain 2 and 4 tightly twisted wires respectively, are commonly used in neuroscience and provide examples of the value that close-packed recordings can have, even when small-scale: such spatial oversampling helps greatly with the "spike sorting" problem in which recorded electrical events are attributed to individual neurons [3],[4]. Silicon based microelectrodes, developed over the past few decades [5]–[8], have recently been designed to include denser arrays of electrodes than in the past [9]–[11], including active probes with the ability to record a subset of points from a dense array [12]–[15]. In this paper, we demonstrate a close-packed silicon microelectrode technology that enables a tight continuum of recording sites along the length of the shank, rather than discrete arrangements of tetrode-style pads or widely spaced sites. This arrangement thus enables tetrode-like spatial oversampling continuously running down the shank, so that separation of spikes recorded by such densely packed electrodes can be facilitated for all the sites of the probe simultaneously. We use advanced lithography tools to create these close-packed arrangements in a scalable fashion, demonstrating probes with 1000 electrode pads situated on 5 shanks with 200 recording sites per shank. A key challenge with traditional silicon electrode designs has been that wiring to the recording sites occupied a large fraction of the available shank area. This is problematic because scaling up the number of recording sites forces the shank geometry to widen, placing an upper bound on the number of sites practical for a single shank of a given width. We here reduced the wire geometry, and thus the overhead that the wiring places on the shank width, by creating submicron wires with high-speed electron beam lithography (EBL). Contact mask lithography enables us to create feature sizes of 2 μm, while in contrast our EBL feature sizes are 200 nm. This gives us an order of magnitude increase in the number of wires for a given shank width. The accuracy of this technology also enables a ~1.5 μm space between individual recording sites, resulting in a close-packed design in a simple single-metal layer process (examples in Figs. 1 and 2). The current paper focuses on principles and fabrication strategies for scale, but does not focus on critical steps that would be needed (for example, specialized coatings) for long-term recording. Our probes may help achieve tetrode-like recordings in large volumes of brain tissue, and may also be useful for investigating the fundamental limits of accuracy and yield of neural recording achievable by electrodes *in vivo*.

II. Process Flow

A. Substrate Choice

The fabrication of our devices was carried out on 150 mm silicon-on-insulator (SOI) wafers (Ultrasil Corp., Hayward CA). The top ("device") layer thickness of the SOI wafer defines the probe shank thickness, and therefore a wide range of precise thicknesses is possible. We chose a thickness of 15 μm, comparable to typical silicon-based electrodes [16]. The device layer is low-resistivity silicon (<0.005 Ω-cm) to help reduce artifacts associated with ambient light. Standard silicon wafers, typically with a resistivity of 10 Ω-cm, have charge

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carrier lifetimes on the order of 1 ms. Even though the wiring is insulated and not in direct contact with the silicon substrate, signals may suffer indirectly from light-artifacts caused by the interaction of charge pairs generated in the silicon substrate with ions in the electrolyte around the shank (for probes from a 10 Ω-cm resistivity wafer, >100 μV_{rms} noise was observed even in ambient room light). This artifact is likely caused by the unequal diffusion coefficients for charge carriers, with resulting charge dipoles arising in response to light. In contrast, carrier lifetimes for the low-resistivity wafers we are using are on the order of 10 ns [17]. The ultra-short lifetimes in low-resistivity silicon ensure that carrier recombination occurs quickly and results in time- and diffusion length-scales irrelevant for an impact on neural signals. In these probes, amient room light can be present without any changes in the noise amplitude.

B. Fabrication Steps: Metallization

The process cross-section and the process flow are shown in Fig. 3. The process consists of two key parts: first, the formation of the insulated metal wiring and exposed metal pads, and second, the deep reactive ion etching (DRIE) steps that define the shape of the probe and the thin shanks.

Fabrication starts (Fig. 3, Step 2) on the double sided polished SOI wafers with deposition of an insulating dielectric (1 μm of Plasma Enhanced Chemical Vapor Deposition (PECVD) deposited SiO_2). We then use electron beam lithography (Elionix ELS-F125, with a 125 kV acceleration voltage) to define the recording sites and high density metal wiring (Figs. 3 and 4). Exposure and development of electron beam lithography resist (400 nm of Polymethyl Methacrylate (PMMA) 495A8 from MicroChem Corp., developed with 1:3 MIBK:IPA) is followed by metal evaporation of a film stack of 10 nm Ti, 150 nm Au, and 5 nm Ti, where the Au is the conductor and the Ti serves as an adhesion layer to the SiO_2 (Fig 3, Step 3). After a liftoff procedure in acetone, a second metallization step follows, using standard optical (UV) contact lithography with a 2 μm feature size. This step (Fig 3, Step 4) uses an image reversal resist (1.5 μm of AZ5214E) and metal for liftoff is deposited by evaporating a 10 nm Ti, 250 nm Au, and 5 nm Ti film stack. Metal liftoff is again performed in acetone. To facilitate the acetone access beneath the photoresist in liftoff, the mask pattern also contains dummy metal filler-shapes (visible in Fig. 7, as 50 μm squares at a 190 μm pitch) in areas of the wafer that are not part of the devices. This helps to break up large unexposed areas that would be more challenging to liftoff.

We adapted a hybrid lithography method, using electron beam lithography (EBL) to write the fine structures on the probes (for example, the finest wiring along the implanted component) while using classical MEMS fabrication techniques for larger structures (for example, the wirebond pads, the non-fine wiring, and the cutout of the probes). Hybrid lithography methods have been used in defining submicron electronic devices [18],[19]. Breaking the metallization into these two steps allows us to utilize the submicron capability of electron beam lithography for dense wiring on the shanks, while maintaining the high throughput of optical lithography to define the less dense wiring outside of the shanks. This helps to minimize the EBL write time needed. The highest wiring density is required when routing alongside the recording sites, because here the shank needs to accommodate both the

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wiring as well as the recording sites, while remaining as narrow as possible to reduce brain displacement or damage. Once the wiring leaves the shank and enters the main body of the probe, significantly more space is available and the wiring pitch can be relaxed, and transitioned to optical lithography (Fig. 4). The EBL exposure itself is broken up into two different write currents, a lower beam current for the smallest geometries on the shank (8 nA for 200 nm wires), followed by a higher beam current for faster writing of wider wires (40 nA for 500 nm wires) used for spreading out to meet the optical lithography patterns. This concept is outlined in Fig. 4, along with the design schematic for a 1000 channel probe. We will discuss the packaging in more detail later, but for optimal packaging, the wirebond pads have been distributed in a comb shape to minimize the size of the silicon chip. The transition from EBL to optical lithography requires a landing pad shown in Fig. 4 (we used a generously sized row of 8 μm pads at a 12 μm pitch). This adds robustness against misalignment that could otherwise result in open circuits in the wiring. Similarly, in transitioning from the 8 nA to 40 nA beam current features, small landing pads (2.4 μm squares set at a 3.5 μm pitch) are used to protect against any position drift during the EBL exposure. This is important, since the EBL exposure writes all shapes of one current level first before writing the remaining shapes of the next current level, and stitching errors between the two current levels can otherwise cause open circuits. Overall, a 150 mm wafer required about 4 to 5 hours of EBL tool time to complete, with approximately 6000 recording sites spread across a variety of different probe styles of 64, 128, 256 and 1000 channels.

After the metal processing on the front side, an SiO_2 layer is deposited and patterned to expose only the recording sites while insulating the wiring (Fig 3, Step 5). We use PECVD SiO_2 films from Tetraethyl Orthosilicate (TEOS) as a silicon source for this step, to obtain a void-free dielectric filling between the high density wires. To pattern the dielectric layer and to open up the electrode and wirebond sites, we again use a combination of EBL and optical lithography. We first pattern and etch open the recording sites with precisely aligned EBL, while the large wirebond pads are patterned and etched with optical lithography (Fig 3, Steps 6 and 7 respectively). The reason for using EBL for the recording site opening step is the ability to have submicron alignment accuracy to the recording sites, and precise definition of the shapes. This allows us to achieve very densely packed recording sites, with 1 to 2 μm spacing between them. The dielectric etch is performed in an oxide RIE etcher (LAM-590 using a CF_4/CHF_3 plasma, with a 5:3 gas flow ratio, a pressure of 2.8 Torr, and 600 W RF power), and we again use PMMA exposed by EBL as mask material (800 nm of PMMA 495A11 developed in 1:3 MIBK:IPA). While PMMA is often not a suitable dry etching mask, we find that it holds up sufficiently well in the CHF_3/CF_4 plasma, showing around 50 nm/min degradation during a 250 nm/min dielectric etch. The thin Ti adhesion layer on top of the Au pads is readily removed during the over-etching step, exposing the Au pad. The larger wirebond pad openings are created using optical lithography and a positive photoresist (1.0 μm of SPR-700) as mask material, and we use the same oxide RIE etch. Oxygen plasma ashing is used to remove the PMMA as well as the SPR-700 resists after each respective etch step. A cross section of the EBL wiring and recording sites is shown in Fig. 5, and a summary of the different metal wiring and pad types is listed in Table 1.

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C. Fabrication Steps: Micromachining

After the metallization is complete (Fig. 3a), we etch out the probe shapes using two deep reactive ion etch (DRIE) steps, as illustrated in Fig. 3b and 3c. This is done by using a Bosch process DRIE tool (SPTS Rapier). We first pattern the wafer frontside with photoresist (8 μm of AZ4620). Because of the presence of dielectrics on the wafer surface, as well as the buried oxide from the SOI wafer, we perform a sequence of three etches with this mask: we first remove the surface dielectric films (2 μm) using the same oxide RIE etch as before (LAM-590), followed by the DRIE etch of the SOI wafer's thin Si device layer (15 μm). The DRIE etch stops on the SOI wafer's buried oxide layer (0.8 μm). We then remove the exposed buried oxide, again with an RIE etch (LAM-590). This sequence of three different etches (Fig 3, Step 8) is done with a single photoresist as mask, and we subsequently remove the photoresist mask in an oxygen plasma asher (Fig. 3b). To define the probe shape and obtain the thin shanks, we pattern the wafer backside with thick photoresist (10 μm of AZ4620), aligned to the frontside patterns. A backside DRIE etch of the handle wafer (SPTS Rapier) is then carried out to etch through the handle wafer (Fig 3, Step 9). For this, we mount the wafer with its front side onto a carrier wafer using AZ4620 photoresist. The backside etch (Fig. 3c) therefore will stop either on the buried oxide or on the previously etched frontside trenches, where the photoresist from the carrier mounting is providing a barrier. The wafer is released from the handle wafer in acetone, and cleaned of photoresist residues by oxygen plasma ashing (Fig 3, Step 10). The dual-sided DRIE etching allows us to create shanks of precisely defined thickness, as determined by the SOI wafer, and also precisely defined shank outlines, as determined by lithography. The parts of the probe that are not going to be implanted can remain at the original wafer thickness, which facilitates handling and packaging (as seen for example in Fig. 6). Furthermore, the devices remain structurally attached to the wafer through several small breakout beams of 100 μm width (Fig. 7). This allows us to complete all processing and cleaning, and only after removing the wafers from fabrication we detach the devices from the wafer by breaking the beams with tweezers.

An example of a probe fabricated in this manner is shown in Fig. 6, showing an SEM of a 1000 channel probe, and illustrating the results of the dual-sided DRIE process. The base of the probe remains at the original wafer thickness (525 μm), and only the shanks are thinned (15 μm). A portion of the shanks themselves can also remain at full wafer thickness if those sections will not enter the brain. This is optional, but can serve two purposes: first, it can act as an additional spacer, providing a greater distance between the probe body and the recording sites. This can help to reduce space constraints during *in vivo* use and enabling a better visibility during the probe insertion into the brain. Second, the thick portions can help avoid unnecessarily long thinned shanks, which can bend due to thin-film stress. While thin film stresses can always be carefully balanced by using a combination of dielectric films under compressive and tensile stress, avoiding the need to do this balancing simplifies the processing. We have fabricated shanks with lengths up to 7.5 mm (at a thickness of 15 μm), and successfully used these without any difficulties. But, we expect more careful stress balancing is needed for shanks with a more aggressive aspect ratio (either longer than 7.5 mm or thinner than 15 μm).

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III. Design Automation

Many different probe designs can be fabricated in parallel on the same wafer (Fig. 8). To create a large variety of unique designs, we automated not only the creation of individual designs, but also the compilation of them into the mask set for an entire wafer. We generate all of the layout drawings with the Cadence Virtuoso CAD design environment. The designs are programmatically generated based on a list of input parameters, using the Cadence "SKILL" programming language to calculate and draw the actual shapes. Fig. 9 shows the design process flow. We have automated the drawing of the individual probe designs ("cells"), but use an additional layer of abstraction by adding a wrapper cell that is able to interpret a set of instructions and generate specific probe designs from it. This wrapper creates all of the different designs and automatically places them into the wafer shape, adding relevant structures for processing such as mask alignment marks or test structures to monitor process performance. It achieves complete automation on the Cadence CAD side, from taking a list of devices and their input parameters, to creating and positioning them into a mask set. The inputs to this automation are collected in a spreadsheet, which administers the default parameters and how to modify specific parameter subsets in order to create a range of designs. This abstraction allows us to drive all the design decisions from a single page, because it contains only those parameters that are modified from their default values. Because most design parameters rarely deviate from their defaults (for example wire width, wirebond pad dimensions, size of buffer regions, and so on), only several key parameters are modified between different devices (for example, the number of shanks, the shank length, or the electrode site pitch). A script code in the spreadsheet then generates and exports the instruction file, which lists the input parameters for each device instance to be created. This instruction file is imported by the Cadence wrapper code, and used in instantiating the different designs. Finally, to move the layout towards fabrication, we perform a final step of layer generation, inserting dummy fillers to help the metal liftoff mask, and export the design from Cadence. The electron beam lithography (EBL) files are generated with the Genisys Beamer conversion software.

The design automation and ease of design entry provide a simple method to modify probe designs or create large varieties of layouts customized to specific target applications. We used this flexibility to create probes with channel counts ranging from 64 to 1000, and also to explore a number of different recording site configurations, which we will analyze in the discussion section.

IV. Device Packaging

To acquire neural signals recorded with the probes, we need to package and connect the probes to electronic amplifiers and digitizers, which are commonly referred to as "headstages". A variety of different systems exist for this task [20]. We utilized headstages with Intan Technologies' RHD2132 amplifiers connected to a recording system as described in the companion paper [21]. The purpose of the packaging is to provide the intermediary routing between the silicon probe and the headstages, and to protect the fragile silicon shanks by providing a mechanical body for handling. Both of these goals are achieved through the use of printed circuit boards (PCBs). We recognize that alternative packaging

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approaches exist that can allow silicon probes to be used for example in freely-moving electrophysiology setups as well [22]. Such approaches are compatible with our silicon technology, and if needed can be implemented in the future.

We directly attach the probes onto a PCB and connect to the probe's wirebond pads using a gold ball bonder (Kulicke and Soffa 4124). To allow wirebonding, the PCB has an electroless nickel immersion gold finish (ENIG). Fig. 10 lists the packaging steps and shows photographs of packaged 64 and 1000 channel probes as examples. While the 1000 channel probe consists of 5 shanks with 200 sites each, for layout simplicity the wirebond pattern uses 1024 pads. Thus, 24 wirebond pads are unconnected to any recording site on the shanks. We used a multilayer PCB to achieve a dense routing of the signals (10 layers, with 8 inner routing layers and 3 mil feature sizes, Advanced Circuits, Aurora CO). These specifications allow us to connect the very densely laid out wirebond pads on the 1000 channel probe. However, for the PCB design, the bottleneck in the layout is the diameter of the via that connects the surface pads to the individual routing layers (in our design, a 14 mil diameter ring with a 4 mil via hole). These dimensions constrained our wirebond pad pitch to 10 mil. Using a more aggressive (albeit more expensive) PCB technology can help reduce this pitch as needed, enabling either higher channel counts or reducing the chip size. However, with our choice of dimensions we find an adequate tradeoff between PCB cost and the required probe size for 1000 channels.

Because the metal we wirebond to on the probe is thin, with only 250 nm of gold, and because it sits on top of a relatively thin layer of 1 μm SiO_2, choosing the right wirebonder settings is important to avoid cratering through the oxide and short circuiting the pads. Typical chip pads in the semiconductor industry often employ a much thicker metal and dielectric stack that is more robust. However, by appropriately choosing the wirebonding conditions (in our case, power and time settings), we found that we can reliably bond all 1000 channels without any pad damage.

The detailed routing scheme of the 1024 channel PCB is shown in Fig. 11. Rather than using a single silicon beam with wirebond columns along its side, as we do for lower channel count designs (as seen in Figs. 8 and 10), for the 1000 channel design we chose to use a multi-column comb-shape layout. This allows us to use a multi-column grid of wirebond pads, reducing the longest wire required on the silicon probe, and also maintaining a more even aspect ratio of the silicon, making it easier to fit the design on the wafer. As the layout in Fig. 11 indicates, the wirebond pads are placed in the gaps of the silicon comb structure, and then connect to the PCB routing layers through vias. The routing across 8 layers in the PCB then takes place below the silicon chip. A photograph of a wirebonded 1000 channel probe is shown in Fig. 11, as well as partially in Fig. 6. While lower channel count probes do not require this many PCB layers, we fabricated them on the same PCB run and therefore benefit from the reduced amount of space needed for PCB routing. The 64 channel probe seen in Fig. 10 illustrates the small form factor that can be achieved. Once the PCB wiring exits the immediate area around the probe, the wiring density can be relaxed as we route towards Flat Flexible Cable (FFC) connectors (Molex 5025983393) that attach to the amplifier headstages. Headstage amplifier circuits can be directly attached to the PCB, for example as in [9],[10], but we decided to use a modular approach in this work to facilitate

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testing of different probe and PCB designs, while preserving the headstage amplifiers in case of probe damage due to user error. We chose FFC connectors for this design because of the low cost and the ability to use flexible cables that help to mechanically decouple the probe from the headstages. But, many other high-density connector types exist, and they can readily be substituted for the FFC connectors. The additional space overhead is acceptable for the acute, head-fixed *in vivo* experiments that we are targeting with this technology, for example for mice in a head-fixed virtual reality environment [23].

For a fully assembled 1000 channel probe, we have measured and listed the parasitic capacitances in Table 2. These are values between adjacent wires, and we chose the worst-case of each of the different design components. However, it is important to realize that adjacent wires on the probe do not necessarily also have to be adjacent on the PCB or the FFC cable. On the PCB, we can therefore significantly reduce the parasitic capacitances, if needed, by periodically shifting the wiring so that any two wires are never adjacent to each other for too long. This effectively could distribute the parasitic capacitance and reduces the worst-case value. Overall, the parasitic capacitances are small when compared to the electrode impedance and the amplifier input capacitance (for example, 12 pF for the Intan Technologies RHD2132 amplifiers chips we are using for the headstages).

We post all code, design files, mask layouts, PCB layouts, and images for this paper at http://scalablephysiology.org/probes/

V. Results and Characterization

To demonstrate the recording capability of the close-packed sites, we have performed *in vivo* recordings in the sensory cortex of an anesthetized mouse. *In vivo* experiments were done in accordance with MIT Committee on Animal Care (CAC) approved protocols. An example of data collected with a single-shank probe bearing 64 pads is shown in Fig. 12. The data illustrates the ability of close-packed recording sites to spatially oversample neural activity, and it shows how activity from the same neuron is picked up by several neighboring sites in its vicinity.

The devices we fabricated have a standard recording site of 9 × 9 μm. We wanted to understand how the dimensions of a recording site impact its electrical properties. For this, we characterized the electrode impedance and the electrical noise as a function of recording site size. The data was collected from single shank 64-channel probes with electrode site dimensions ranging from 2.4 to 9.6 μm. We gold electroplated each recording site with a constant current density protocol (60 pulses of 1-second at 0.1975 nA/μm^2).

Fig. 13 shows the magnitude of the recording site impedance, measured at 1 kHz in 0.9% saline. As the electrode dimensions increase, the impedance decreases. We can think of the electrode impedance as a parallel combination of unit impedances. This would suggest that the impedance is inversely proportional to the electrode site area, which we observe in the data of Fig. 13. However, we expect mass transport limitations to eventually impact this scaling behavior [24],[25], and therefore would caution against extrapolating the data beyond what was measured, on the basis of area alone.

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We also characterized the electrical noise of the recording sites. For this, we inserted the probe into saline, and using a wire in the saline as reference ground, recorded all 64 channels in parallel. We calculated the root-mean-square (RMS) noise voltage in the 50 Hz to 15 kHz frequency band. The noise spectrum was verified to be free from 60 Hz pickup or its harmonics. We expect the noise to depend on the electrical properties of the electrode site [26],[27]. Fig. 14 shows the measured RMS noise as a function of the electrode site impedance.

From the data in both Figs. 13 and 14, we recognize that the 9 μm × 9 μm recording sites can, in principle, be reduced significantly to build probes with smaller form factors or even denser arrangements of recording sites. For example, the data suggests that even a 3 μm × 3 μm site has electrical characteristics compatible with recording single unit activity, with impedances of 2 MΩ and a noise level of 8 μV_{rms}.

VI. Conclusion

We have introduced a platform to fabricate close-packed microelectrodes for neural recordings, and described the design, fabrication, and packaging methods that allow us to create a large range of scalable probe designs with close-packed recording sites. Although multisite silicon probes have been generated before, as noted in the introduction, the hybrid fabrication method here enables us uniquely to pursue electrode spacings far denser than in earlier implantable probes, thus enabling the feature of spatial oversampling of the neurons. The *in vivo* experiment and quantitative electrode site impedance and noise characterization demonstrated that by closely packing recording sites, we are able to spatially oversample and pick up unit activity on several recording sites at a time, and that the size of the recording sites can be reduced even lower than 9 μm. Our results suggest that close-packed electrodes may become not only instrumental for neuroscience, but also for understanding basic principles of electrode design when scaling to large channel counts is required. We note that our current technologies are not designed for long-term recording, which may benefit from probes that are coated with alternative materials [28], as well as thinner probes that may be more flexible [29]; our main focus here was on the principles of scalability, as well as acute recordings. Future work may enable such scalable devices to be deployed in chronic as well as acute settings.

Acknowledgments

This work was supported by the Simons Center for the Social Brain at MIT, the Paul Allen Family Foundation, NIH Director's Pioneer Award DP1NS087724, NIH grants R01NS067199, 2R44NS070453-03A1 and R01DA029639, Cognitive Rhythms Collaborative NSF DMS 1042134, IET Harvey Prize, Google, New York Stem Cell Foundation, NSF CBET 1053233, and DARPA HR0011-14-2-0004.

Devices were fabricated at MIT's Microsystems Technology Laboratories (MTL). DRIE etching was carried out at the Harvard Center for Nanoscale Systems (CNS), a member of the National Nanotechnology Infrastructure Network (NNIN).

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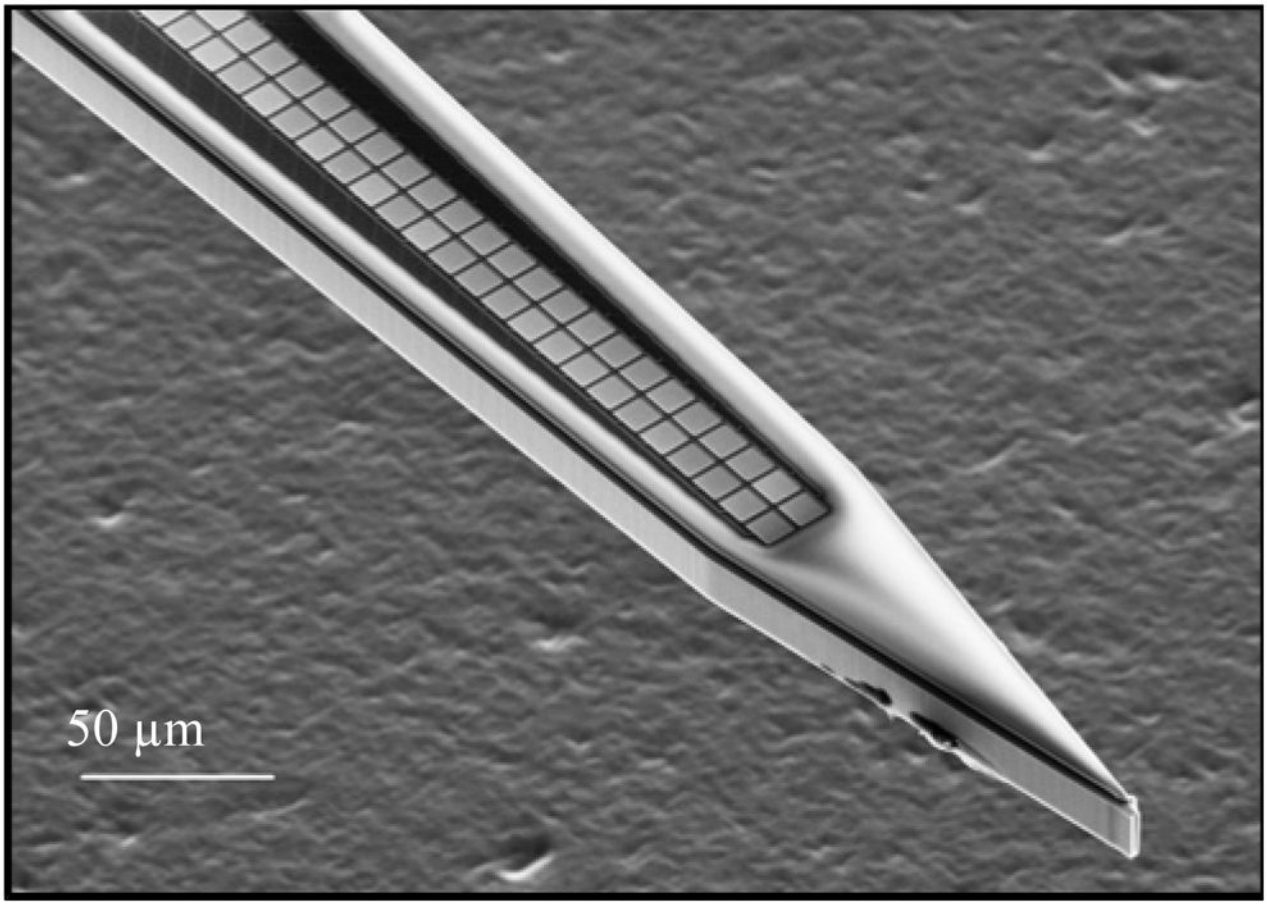

Fig. 1.

Close-packed recording sites on a silicon shank, for spatially oversampled neural recording. Scanning electron micrograph (SEM) of the tip of a recording shank with two columns of 100 rows each. The close-packed recording sites of 9 × 9 µm have a pitch of 11 µm, and are visible as the light squares. Insulated metal routing runs along the length of the shank, visible as dark lines flanking the rows of light squares. The shank itself has a width of ~50 µm in the region shown, and is 15 µm thick.

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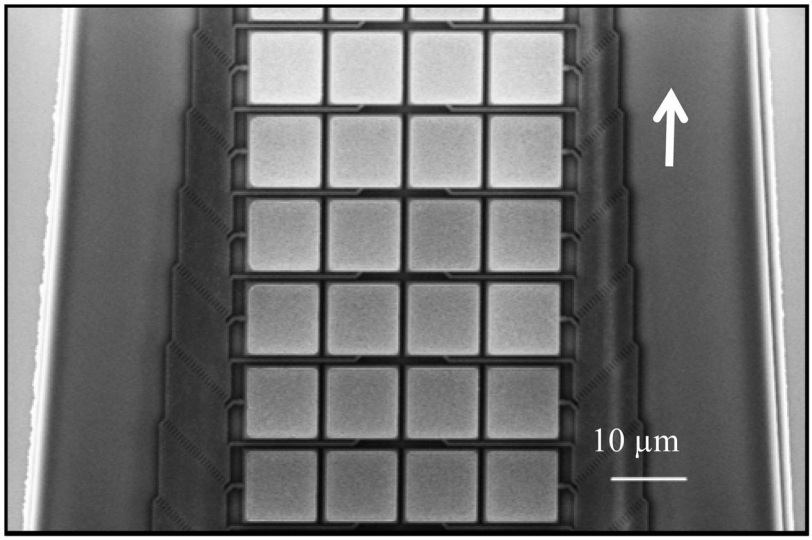

Fig. 2.

Top-down SEM view of a four-column shank of close-packed electrodes. The center columns are connected by wiring running in-between the outer pads, and all columns are then collected and routed along the two sides. The direction towards the shank tip is indicated by the arrow.

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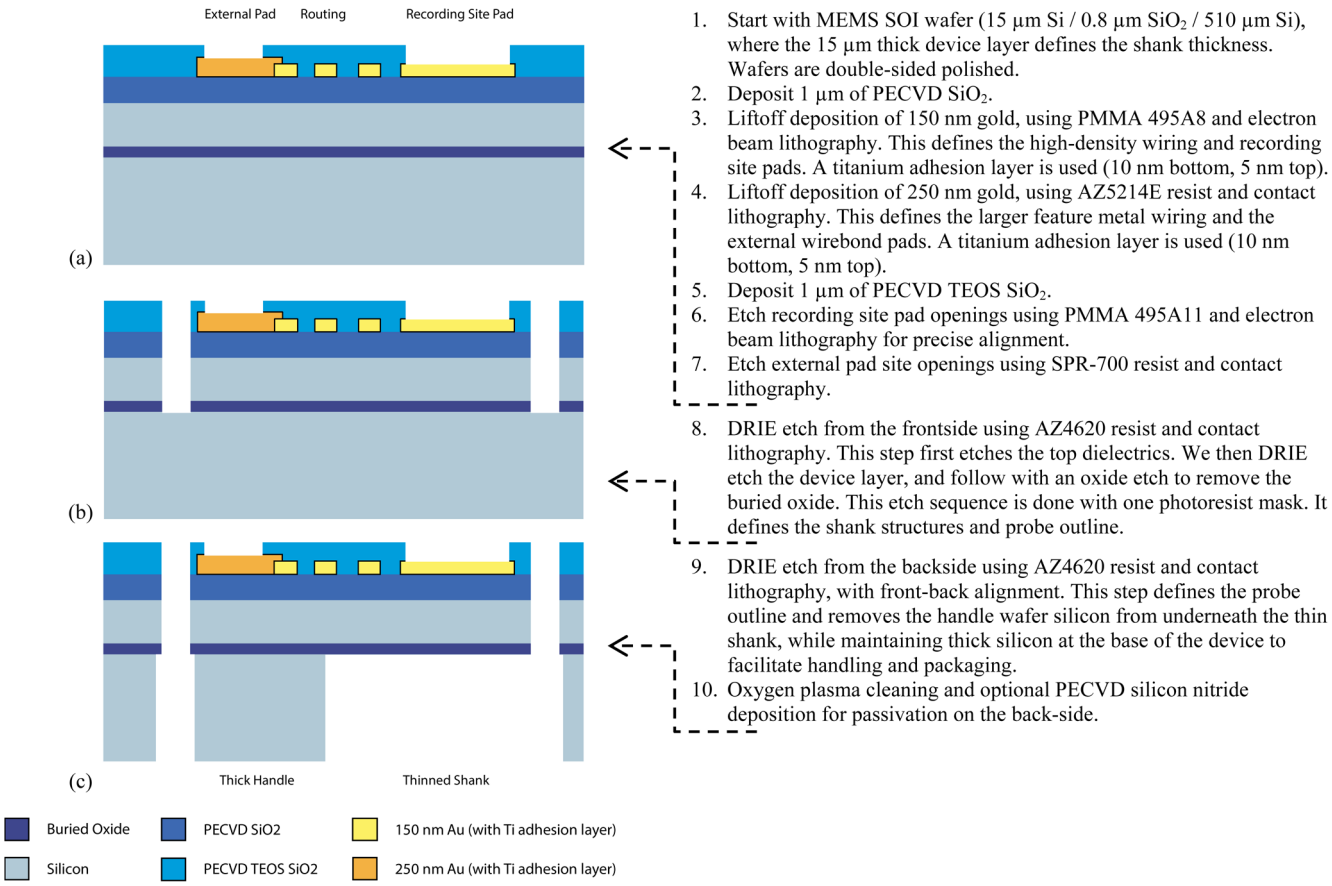

Fig. 3.

Simplified process cross-sections (not to scale) during key steps of the fabrication process: (a) metallization, using two different metal deposition steps, (b) front- and (c) back-side DRIE etches that define the probe shape. The shank thickness is determined by the choice of SOI device layer thickness. The process details are shown in the list on the right. The arrows indicate between which process step the cross sections correspond to. Final devices and actual cross-sections are shown in Figs. 5 and 6.

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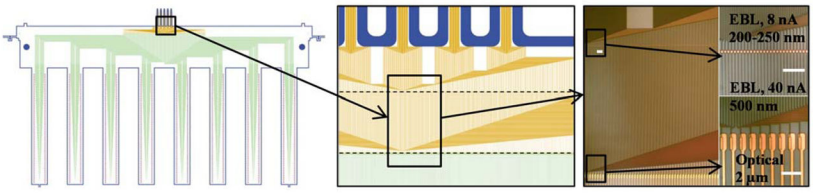

Fig. 4.

To route the high-density wiring from the recording sites (as shown in Fig. 1) to the large wirebond pads on the probe periphery, we use a combination of electron beam lithography (EBL) and contact (optical) lithography. The left drawing shows the 1000 channel probe's routing scheme, from the recording sites at the very top to the wirebond pads on the bottom. EBL wiring on the probe shanks (yellow) connects to contact lithography wiring on the base of the probe (green). The center drawing shows the transitions from 8 nA to 40 nA beam currents, as well as from the 40 nA EBL to contact lithography, with the two transitions marked by dashed lines. To be able to handle alignment errors and possible wafer drift during long EBL writes, these transition regions consist of a larger landing pattern, as indicated by insets in the microscope images on the right. The white scale bars correspond to 25 µm.

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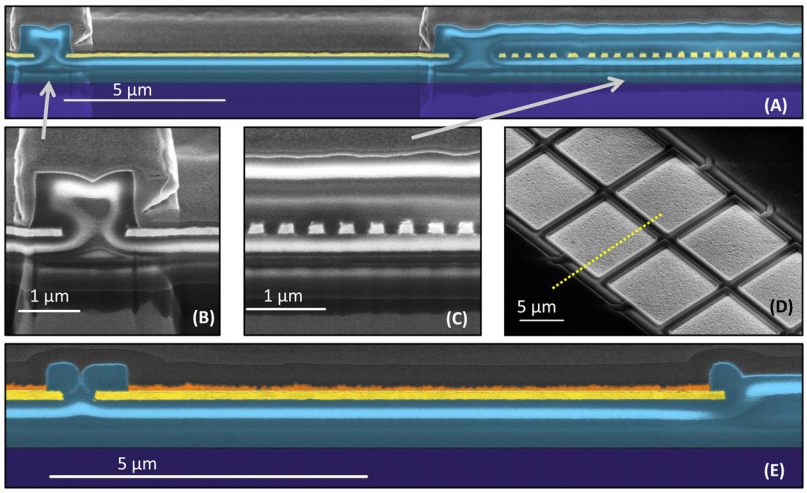

Fig. 5.

SEM and cross section images obtained by focused ion beam (FIB), showing the metallization and recording sites. (A): an 11 µm recording site with high density wiring adjacent to it, in false color. The gold metal is shown as yellow, and comprises both the recording site and the wiring. The TEOS SiO_2, shown in cyan, provides a smooth and void-free insulation layer. The silicon substrate is shown as dark blue. (B): close-up of the contact etch between two adjacent recording sites. A mild lithography misalignment of around 150 nm is noted, and the layout was designed to be indifferent against such misalignments. (C): close-up of the high density wiring where wires are 200 nm wide, placed at a 400 nm pitch, and 150 nm thick. (D): SEM of the top view of a two-column recording shank, showing the close-packed recording sites, and the wiring on the sides. The orientation of the cross sections in this figure is indicated by the dotted line. (E): a 9 µm recording site, after surface preparation by gold electroplating. False coloring used as previously in (A), but the additional electroplated gold layer (shown as orange) is visible and its surface roughness helps to lower the electrode site impedance.

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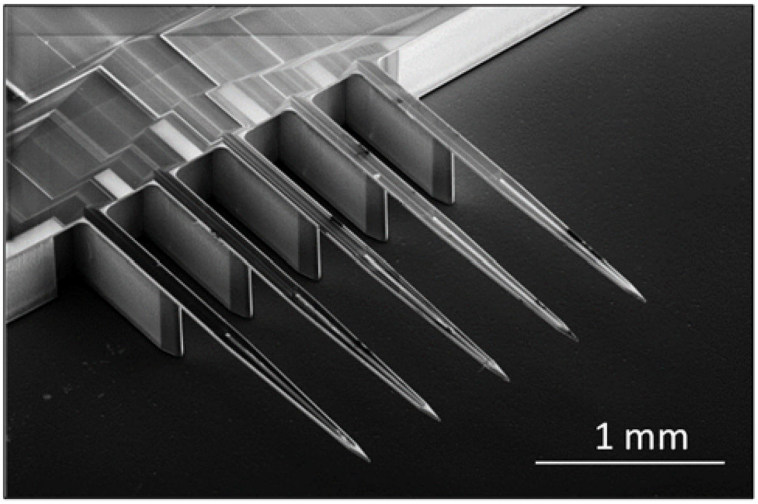

Fig. 6.

SEM view of a 5 shank, 1000 channel probe fabricated with the process shown in Fig. 3. The 15 μm thin shanks and thicker support structures are visible. The handle wafer thickness is 510 μm, and the device layer is 15 μm. The buried oxide is 0.8 μm, sufficiently thick to serve as a DRIE etch stop during the through-wafer backside etch, but thin enough to remove easily after the frontside etch. The shanks have a pitch of 500 μm. The tip portion of one shank is shown in Fig. 1.

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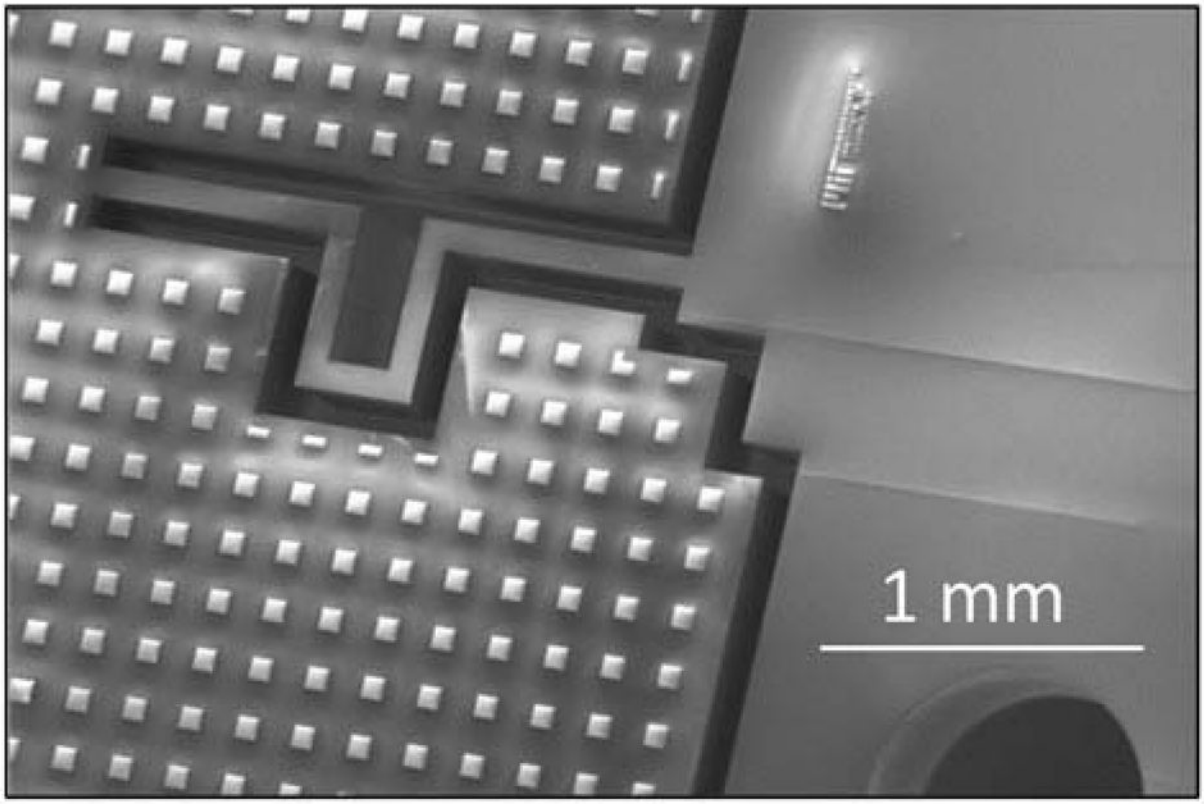

Fig. 7.

SEM view of the breakout beams that connect the side of the 1000 channel probe (right half of the image) to the bulk of the wafer (left half of the image). These beams, also visible in Fig. 8, are sufficiently strong to allow wafer handling during the last process steps without accidental breakage (unless the wafer receives a sharp shock), but weak enough to easily break with tweezers or a needle point. A wide range of beam designs are sufficient for this, but we used a U-shape bend to allow an easy access point for breaking the beams. Also visible are metal filler structures on the left, outside the probe, to facilitate the metal liftoff procedure.

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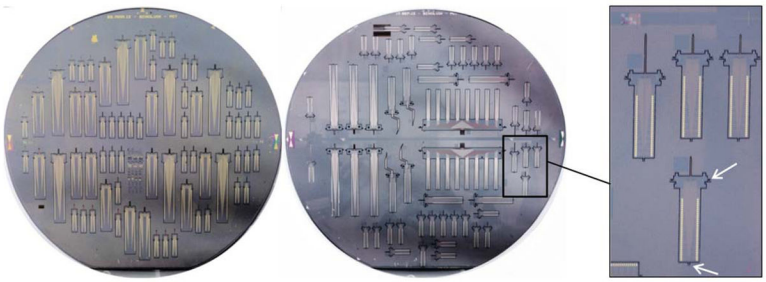

Fig. 8.

Photographs of two wafers illustrating a large variety of designs, with probes ranging from 64 to 1000 channels. All of these devices were created automatically by parameterized cells and arranged on the wafer algorithmically. The devices in the right wafer are aligned to have the shanks point towards the wafer center, in order to avoid yield drops in the electron beam lithography that can occur close to the wafer edge. The close-up on the far right shows a section of the wafer with four 64-channel test probes. Each of these probes has different characteristics, such as the shank length or variations in recording site dimensions. A set of small breakout beams hold the otherwise released probe in place on the wafer (seen as small notches, on the bottom of the probe as well as the left and right sides on the top, identified by white arrows). Fig. 7 shows a breakout beam used in the 1000 channel design in more detail.

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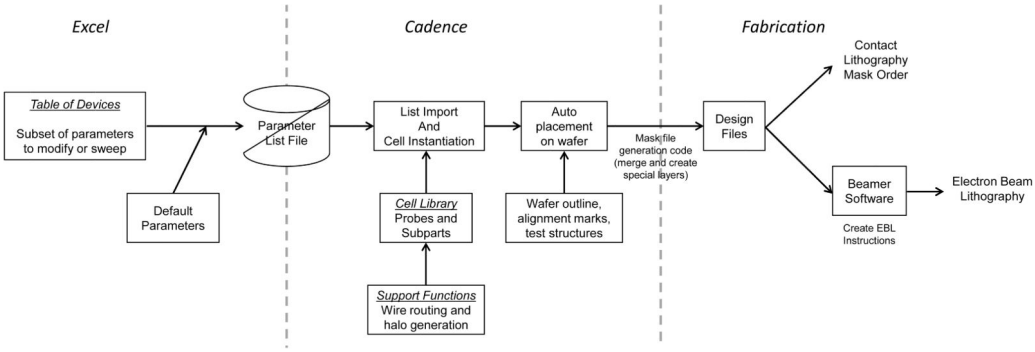

Fig. 9.

Components of the design automation: Design parameters are entered by the user in a spreadsheet, exported along with default values for any unspecified parameters, read in by a Cadence script, and automatically processed to generate all of the designs and arrange them on the wafer area.

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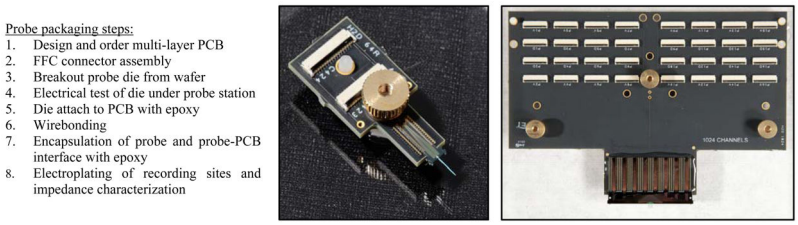

Fig. 10.

Summary list (left) of the probe packaging steps, and images (center, right) of packaged probes. Electrical testing before die assembly verifies that the probe shank wiring is intact, by measuring the roundtrip resistance between two wirebond pads short-circuited at the recording sites. Center: Example of a 64-channel probe with a 5 mm long shank, held inside a plastic box for transport, using nylon threaded standoffs and thumb nuts. The PCB is assembled with the FFC connectors, and then the probe is attached and wirebonded. The photo is prior to encapsulating the probe wirebonds with an epoxy that insulates it against liquids. Right: the 1000 channel probe follows the same principle, but uses a larger PCB with 32 FFC connectors. Encapsulation was done with a clear epoxy (Loctite M-31CL).

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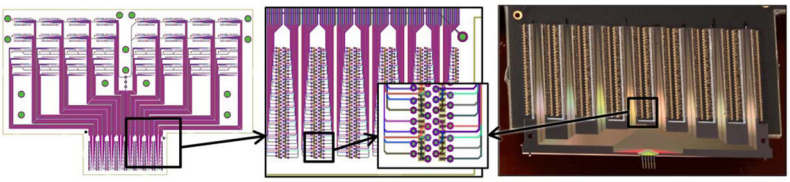

Fig. 11.

PCB design schematics for the 1000-channel probe. Instead of routing the wirebonds out in a two-column bar, as done in the 64-channel probe, we break up the routing for the 1000-channel probe into a comb-shaped multi-finger design, of 8 fingers with 128 pads each (photograph of the probe after wirebonding but before encapsulation). This allows us to maintain a better aspect ratio of the silicon, and then route the wiring on the PCB across 8 inner layers to the connectors seen at the top of the schematic.

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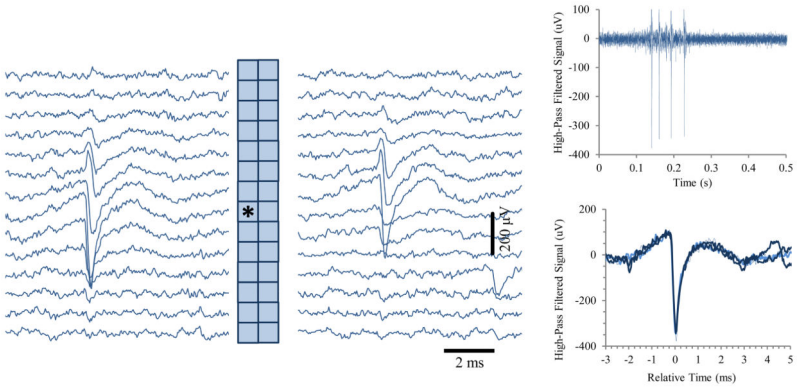

Fig. 12.

In vivo recordings with a close-packed electrode array in the sensory cortex of a head-fixed mouse under light (0.5%) isoflurane anesthesia. Left: example of the recorded data for a single spike across 28 pads (2 columns of 14 rows) on a 64-channel probe. Our spatial oversampling design enables the spike to be picked up by several nearby recording sites (9 × 9 μm pads, 10.5 μm pitch). The vertical scale bar is 200 μV. Right: Focusing on a single recording site (marked with a star in the probe map on the left), four consecutive spikes (top) are then overlaid (bottom) to show the spikes in more detail.

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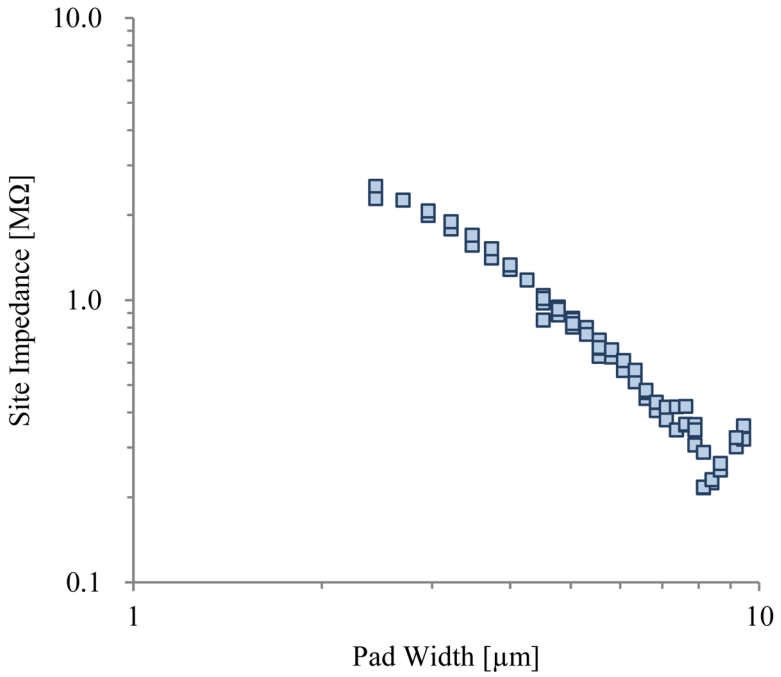

Fig. 13.

Electrode site characterization as a function of electrode dimensions for square pad sites. The electrode impedance into saline was measured at 1 kHz, and the magnitude of the complex impedance is shown. The probes were gold electroplated with a total charge of 11.85 μA-s/μm^2, spread out across 60 pulses of 1 second duration each. As the pad size increases, the impedance drops. Even for pads as small as 3 μm × 3 μm, the electrode impedance is 2 M or less. For the 9 μm × 9 μm standard recording sites used in the closely packed probes, low impedances between 0.3 to 0.6 M are observed.

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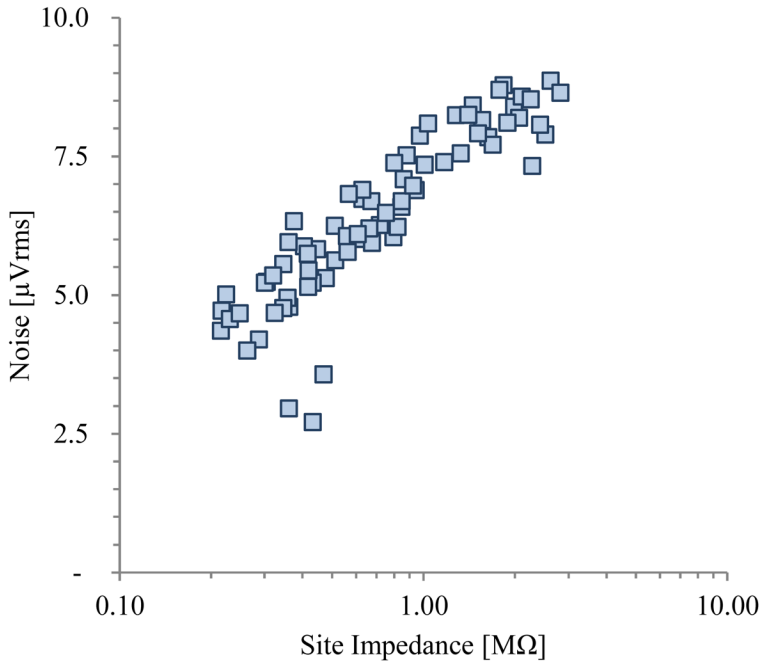

Fig. 14.

Electrical noise measurement as a function of electrode impedance for the same sites as shown in Fig. 13. The contribution of input referred noise from the amplifiers (2.4 μV_{rms}) was removed from the data.

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TABLE I

Lithography and Dimensions

Wiring Element	Line Width	Line Pitch	Length Range	Lithography Details
Routing next to recording sites	0.2 µm	0.4 µm	0.1 – 1.2 mm	PMMA, 125 kV, 8 nA
Dense wiring up the shank	0.25 µm	0.5 µm	1 – 8 mm	PMMA, 125 kV, 8 nA
Distribution on the probe base	0.5 µm	1 – 12 µm	0.6 – 5.9 mm	PMMA, 125 kV, 40 nA
Routing to wirebond pads	2 – 5 µm	4 – 12 µm	2 – 34 mm	AZ5241E

Pad Element	Pad Size	Pad Pitch	Lithography Details
Recording site	9 × 9 µm	10.5 – 11.5 µm	PMMA, 125kV, 8 nA
Wirebond pads	250 × 125 µm	250 µm	AZ5241E

Summary of the lithography wiring and pad types, and their geometry. Wiring lengths depend on the probe geometry and the position within the probe design (wiring on the outer edges can be much longer).

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TABLE II

Overview of Wiring Parasitics

Component	Measured	Wire Length
1000-Channel, PCB Parallel Wire Capacitance	7.2 pF	127 mm
1000-Channel, Probe Parallel Wire Capacitance	4.9 pF	43 mm
1000-Channel, Probe Line Resistance	8.7 kΩ	43 mm
64-Channel, PCB Parallel Wire Capacitance	2.1 pF	41 mm
64-Channel, Probe Parallel Wire Capacitance	2.4 pF	14 mm
64-Channel, Probe Line Resistance	3.5 kΩ	14 mm
FFC Cable, Parallel Wire Capacitance	3.8 pF	100 mm
FFC Connector, Parallel Pin Capacitance	0.5 pF	n/a

Comparison of the sources of worst-case parasitic capacitances and line resistances for 64- and 1000-channel probes as well as the corresponding PCBs. The PCB has a 3 mil line and space, and 6.5 mil vertical pitch between different layers.