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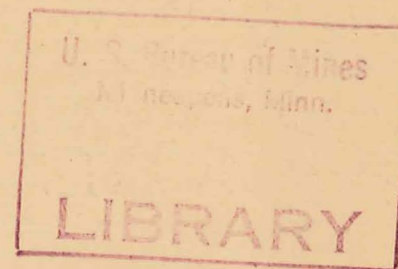
TIME DOMAIN REFLECTOMETRY MICROCOMPUTER

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BUREAU OF MINES

by

CARNEGIE-MELLON UNIVERSITY
ELECTRICAL ENGINEERING DEPARTMENT
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January, 1975 to March, 1977

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CABLE FAULT LOCATION AT ELEVATED VOLTAGE LEVEL

March, 1977

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16. Abstract This report describes in detail the work done on the development of the Time Domain Reflectometry Microcomputer (TDRM). Modifications to the FMC- Model 302A Cable Fault Locator is described in Appendix D. The TDRM unit uses an 8080 microcomputer to accurately locate major faults in low capacitance cables to within ± 1 foot when properly calibrated. Major faults in high capacitance cables are usually located within ± 5 feet. The upper limits of fault detection are <1 kilohm shunt fault and >7 ohm series fault. In practice fault detection limits are reduced to <300 ohms shunt fault and >30 ohms series fault because of discontinuities caused by cable repair.			
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- FOREWORD -

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This report is a summary of the work recently completed as part of this contract during the period January 1975 to March, 1977. This report was submitted by the authors on March 30, 1977.

1977 ANNUAL REPORT
TIME DOMAIN REFLECTOMETRY MICROCOMPUTER

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INTRODUCTION

Faults which occur in electrical coal mine trailing cables as either short circuits or open circuits have been successfully located in the past by a variety of simple techniques. On the other hand resistive faults require the use of more sophisticated techniques to provide accurate fault location, especially in the range of 50 ohms to 1 megohm.

Generally resistive faults occur because of the rapid action of protective devices which limit discharge energy to the faulted area. Thus visual evidence such as scorch marks, swelling or blowout are not observed. Although a protective device may be set to trip a faulted cable with resistance of 50 to 100 ohms, such resistive faults may resolve themselves into faults approaching 1 megohm or greater, especially if the cable is mechanically flexed or allowed to dry out. Therefore, it is most desirable that the fault be located accurately within the mine with the least disturbance to the cable. Should the faulted cable be removed from the mine and allowed to dry out, it would be advantageous that the same instrument used in the mine for fault location be applicable to above ground usage on faults which may be more difficult to locate.

Among the many methods reviewed, time domain reflectometry has the potential to accurately describe each significant fault location in terms of magnitude and location. The method can also be used with shielded cables where external probe techniques usually fail. Although laboratory type TDR instrumentation has existed for years, its application in the mine was limited by both its incompatibility with a mine environment and the need for operator interpretation of the complex waveforms.

With the introduction of low cost microprocessors, the use of a small portable microcomputer to interpret these waveforms became a possibility. Because the microcomputer can be software programmed through PROM'S (Programmable Read Only Memories), future program changes can be made with little or no hardware changes. Thus future program improvements and in-field corrections to solve certain program problems can be implemented easily. As new algorithms are developed or old ones optimized, the power of software programming becomes obvious.

This part of the report describes in detail the Time Domain Reflectometry Microcomputer (TDRM) developed by Carnegie-Mellon University for the U.S. Bureau of Mines.

Chapter 1

TDRM HARDWARE

This chapter describes the electrical hardware and schematics used in the development of two similar prototypes. The basic difference between the prototypes is the use of two different sample and hold circuits. The first prototype uses the Datel SHM-UH device with 200 picosecond aperture time and 500 V/ μ sec slew rate. The second prototype uses the less expensive Datel SHM-2 device with 10 nanosecond aperture time and 30V/ μ sec slew rate. The second prototype is less accurate than the first because it uses the SHM-2 and does not isolate the sampling circuitry from the computer by use of a separate power supply.

1.1 Hardware System Structure

A block diagram of the hardware used in the prototype is shown in Fig. 1.1. The pulse generator produces a 10 microsecond, 10 volt pulse every 240 microseconds. Pulse rise time is 10 nanoseconds to give a fault location accuracy of approximately 3 feet.

The sampling circuit consists of two analog ramp generators. The fast ramp generator has a period of 240 microseconds while the adjustable slow ramp generator has a nominal period of 1 second. Comparison of the two ramp voltages by an analog comparator, will produce a sampling pulse each time the voltage magnitude of the slow ramp exceeds that of the fast ramp. Thus, the TDR waveform can be broken down into 1000 discrete samples, and each advanced in time by the equivalence of 1 foot in distance.

The sampling circuit also controls the sample/hold (S/H) circuit, the analog to digital converter (A/D) and the 8080 microcomputer. A S/H module with a 200 picosecond aperture time, 35 nanosecond acquisition time and an output slew rate of 500 v/microsecond was chosen for

the initial prototype to avoid slew rate problems. The use of a 10 nanosecond aperture time S/H modules with a reduced output slew rate is used in the second prototype unit.

The analog to digital converter is activated by a pulse from the sampling circuit which occurs just after sample conversion by the S/H circuit. The A/D converter has an eight bit resolution with a 4 microsecond conversion time.

An additional pulse from the sampling circuitry is used by the computer to initiate the start of the sampling period. This pulse is necessary to prevent false recording of the fast return pulse of the slow ramp generator.

An 8080 microcomputer was chosen for the TDRM for several reasons: programming capability, years of field experience, and 8 bit data capability. With the many new microcomputers available today any other equivalent microprocessor could also be used. The 8080 microcomputer operates at a 1.6 microsecond state cycle to accommodate data transfer from the slow PROM memories. 1K of program memory is used with 1K of RAM (Random Access Memory) to perform all necessary functions of the TDRM. An additional 1K of RAM is available for program expansion. Two eight bit input ports and 1 eight bit output port are used by the computer for external control and input/output.

A mode control switch selects between Match, Detect, Average and Data modes which will be described in the Operation section. In addition a fast advance control is available for use in controlling the display speed in the Data mode.

A time multiplexed display is used to transfer data from the computer to the operator. The display uses numerical light emitting diode

indicators. Fault magnitude and distance to each discontinuity is transferred to the display in the Detect and Average modes.

The layout of controls for the TDRM is shown in Figs. 1.2 and 1.3 for two TDRM prototypes. The unit is packaged in a standard printed circuit card rack assembly complete with all necessary power supplies. The prototype unit operates on 120 volts ac and can be used with a battery pack and simple square-wave ac inverter for portable operation. By use of a special dc-dc power supply, the TDRM unit can be considerably reduced in size from the present prototype size of 19" x 6" x 9".

1.2 The Sampling Circuit

The Sampling Circuit consists of the Timing Circuit, Pulse Generator, Sample/Hold Circuit, Analog/Digital Converter and interface circuitry. The circuit is distributed on two plug-in printed circuit cards. The first card is called the Timing Card which also houses the pulse generator. The second card is called the S/H & A/D Card on which the Sample and Hold and the Analog to Digital Converter Modules are mounted.

1.2a Timing Card

Since the TDR waveform is so short in time with sample points being separated by 2 to 4 nanoseconds, it was necessary to sample 980 separate TDR waveforms to permit sufficient time for microcomputer storing operations. Since each of the 980 TDR waveforms are identical to each other sampling techniques can be used.

The Timing Card (see Fig. 1.4) uses two 8038 ramp generator integrated circuits (I.C.'s) for ramp generation U1 is the fast ramp generator and U4 is the slow ramp generator. As Fig. (1.5) shows, sample points produced by the intersection of the slow ramp with the fast ramp produces a

pulse which appears to advance along the fast ramp. The intersection point is determined by the comparator circuit of U7. Each time the slow ramp exceeds the magnitude of the fast ramp a pulse is produced. This pulse is fed into a monostable flip-flop U5 which produces a short pulse to trigger the Sample/Hold module (SHM-2 or SHM-UH). U5 in turn triggers U6 to produce a triggering pulse for the Analog to Digital Converter.

U1 has a fixed period of 240 μ sec, whereas U4 is controlled externally by means of an external calibrate control to allow for differences in cable phase velocity. The output of U1 is passed into monostable U2 which produces a constant delay of about 75 μ sec to permit operation in the linear region of the ramp generator. The output of U2 feeds monostable U3 which produces a 15 μ sec pulse used for TDR pulse generation. Transistors Q1 and Q2 form the TDR pulse generator and are used with an external Z_0 potentiometer and wave shaper. When properly adjusted pulse rise-times of 10 to 15 nanoseconds are possible with the pulsing circuit.

The only on card adjustment is made by trimpot R_T . This trimpot controls the initial starting point of the sampling pulse on the TDR waveform. R_T is part of a voltage divider which biases the attenuated signal from the slow ramp generator for comparison with the fast ramp.

To prevent the computer from recording TDR values produced by the fast return ramps, a pulse produced by U4 is fed into U8. U8 in turn produces a 200 μ sec Start Sampling Pulse which is used by the microcomputer program to initiate sample storing operations.

Fig. 1.4 shows the +5 volt D.C. power supply being derived from the +15V D.C. power supply through a 5 volt 7805 voltage regulator. Although reasonably effective for use with the SHM-2 sample/hold module, a separate +5V_{DC} and ± 15 V_{DC} are recommended for the sampling circuit. The first

prototype was built with separate power supplies.

Although not shown decoupling capacitors should be appropriately located across each integrated circuit especially at U1, U4 and U7.

1.2b Sample/Hold & Analog/Digital Card

Two versions of this circuit were built. The first prototype uses the Datel SHM-UH shown in Fig. 1.6 and is preferred for best accuracy. The second prototype uses the Datel SHM-2 shown in Fig. 1.7. Since the SHM-2 has a slew rate 15 times slower than the SHM-UH almost 50 sample points are required to reach a steady state value on a 5 volt step TDR waveform. Such slow response causes problems in detection accuracy especially at the beginning of the TDR waveform.

Fig. 1.6 uses an operational amplifier circuit (U2) with a gain of 2 to match the 5 volt SHM-UH output to the ADC-EH8B 10 volt input. U1 is used to increase the end of conversion pulse on time from the ADC-EH8B to 80 μ sec to permit adequate time for microcomputer software operations. The $+5V_{DC}$ and $\pm 15V_{DC}$ power supplies are isolated from the computer power supply to eliminate noise problems.

In Fig. 17 a $+5V_{DC}$ supply is derived from the $+15V_{DC}$ computer power supply. Although operational, separate supplies are recommended as suggested for the Timing Card.

Details on SHM-2, SHM-UH and ADC-EH8B operation are described in the appropriate data sheet which can be obtained from Datel.

1.3 The Display Circuit

One plug-in type card called the Output Decoder-Driver Card and a panel mounted Numerical Display Card make up the display circuit. Fig. 1.8 shows the Output Decoder-Driver Card.

Eight separate Light Emitting Diode (LED) Numerical Displays are used in a multiplexed mode driven by eight separate digit drivers. The digit drivers act under control of U2 to turn on each digit in an order specified by the microcomputer program.

U2 is an 8205 I.C. which accepts a Binary Coded Decimal (BCD) Address from the computer to activate the appropriate digit driver by electrically connecting the selected transistor base drive resistor to ground. When grounded the selected transistor Q1 through Q7 is turned on which in turn activates the proper LED display digit.

U1 is a segment decoder which converts BCD information from the computer into a decimal number. Both BCD address from the computer to select the proper digit and a decimal value encoded in BCD are required to display one decimal number on the LED display.

The output decoder-driver card also houses resistor-diode decoding circuitry for use with the mode control switch. The decoder allows for more efficient use of the computer input ports.

The Numerical Display (Fig. 1.9) consists of 7 numerical MAN 7 LED's (6 for the first prototype) and one matching $\pm$ LED display. All like display segments are wired in parallel with a series 10 Ω segment resistor. Since the display is multiplexed, the segment resistor must be low in value to insure adequate illumination during multiplexing.

Under control of the computer each digit driver turns on digit 8 through digit 1 in a multiplexing operation. Multiplexing control is effected by separately wired LED digit anodes under digit driver control.

Multiplexing is performed at a speed near 1K Hz so that all display digits appear to the human eye to be simultaneously lit.

1.4 The Microcomputer ^{1,2}

A Prolog MPS 883 Microcomputer was chosen for use in the TDRM. The system consists of three cards; the CPU card, the memory card, and the I/O card.

The CPU card utilizes the 8080 microprocessor with a 1.6 μ sec state cycle and reset control. The CPU unit performs the normal computer processing under direction of the other two plug-in cards.

The memory card utilizes four-1702A programmable and ultraviolet light erasable read only memories (PROMs). Since each 1702A holds 256-8 bit words, the memory card is capable of storing up to 1K of programming in PROM. The remaining memory is made up of random access memory (RAM). Eight 2102 RAMs provide 1K of random access memory with an extra 1K of RAM sockets available for expansion.

The input/output (I/O) card provides 28 TTL I/O lines, hardware selectable in groups of four as input gates or output latches.

The MPS 883 is one choice for a microcomputer although any other equivalent microcomputer could be chosen for the TDRM. Choice of a microprocessor other than the 8080 would, of course, require major software reprogramming.

Further details on the MPS 883 can be obtain from PROLOG. The following describes the TDRM utilization of the MPS 883.

Figures 1.10 through 1.12 functionally describe the three microcomputer cards. Figures 1.13 through 1.15 show printed circuit card pin identification. Pins with the same label are to be wired together. Figures 1.13 through 1.15 can be used as a microcomputer interwiring diagram. Both detail schematics and card interwiring are available from

PROLOG and are not reproduced here.

Fig. 1.16 shows the I/O utilization by the TDRM. Connections are made from the TDRM circuitry to the specified pins on the Prolog I/O card.

Port 0 acts as an input port to accept digitized TDR data from the A/D converter. Port 1 acts as an output port to control the display through the output decoder/driver card. Port 3 is a four line input port which receives an X and Y signal from the decoder/driver card to specify the operational modes of Match, Detect, Average, and Data. A third Port 3 input line receives the start of sampling signal from the timing card to indicate the beginning of TDR data. Finally the end of conversion signal from the S/H & A/D card is also received as input to Port 3. One half of Port 2 is used as an input port to direct the computer to increase display speed and to select between two different detect modes as required by a software program used in the second prototype.

1.5 Front Panel Power Supplies, and Component Location

Figure 1.17 shows the front panel and power supply diagram for the TDRM unit. Since the prototype uses A.C. to D.C. power supplies a square wave type inverter with a rechargeable battery can be used for portable operation.

For the second prototype three 15 watt A.C. to D.C. power supplies were used to obtain $+5V_{DC}$ and $+15V_{DC}$. From the $+15V_{DC}$ power supply $+12V_{DC}$ was obtained through a 7812 voltage regulator to drive the PROLOG MPS 883. An adjustable (set to $-10V_{DC}$) negative power supply was obtained from the -15 Volt D.C. through a 7905 voltage regulator circuit.

In the second prototype isolation of the +5 volt supply to the timing card and the S/H & A/D card was obtained by the use of 7805 voltage regulators mounted directly on their respective cards.

The first prototype used all the power supplies shown in Fig. 1.17, and also included an additional $+5V_{DC}$, $+15V_{DC}$ modular power supply to provide isolation.

The front panel controls consists of an On-Off switch, Reset switch, Calibrate potentiometer, Z_o potentiometer, Fast switch, and a Mode switch. The mode switch is relocated on the second prototype to the right thus eliminating the mode indicator lights of the first prototype. (See Figs. 1.2 and 1.3.

The On-Off switch interrupts the $120V_{AC}$ power to the power supplies to turn the unit on or off. The Reset switch is a normally open (N.O.) push button which is wired to PIN 52 of the Prolog MPS 883 CPU card to provide reset control. When the Reset switch is depressed PIN 52 is grounded to effect a program reset.

The Calibrate potentiometer is used with the slow ramp generator on the Timing Card to adjust the sampling rate so that one sample point equals 1 foot. The Calibrate control adjusts for phase velocity differences among the various coal mine trailing cables.

The Z_o control receives the TDR pulse from the Timing Card pulse generator and matches the pulse generator impedance to the cable impedance " Z_o ". The 500Ω Trimpot in series with the 220 pF capacitor are used to optimize pulse risetimes introduced into the trailing cable at approximately 10 nanoseconds.

The Fast switch is a (N.O.) push button wired to ground and to PIN 21 of the I/O card. Depressing the switch produces a low signal at Port 2 terminal 21 to cause a fast display. Although all modes are affected, the pushbutton is to be used in the Data Mode.

The Mode switch is a 6 position 2 pole switch in the second prototype and a 4 position 3 pole switch in the first prototype. The switch grounds the J, K, and L terminals on the Decoder/Driver card to select from the four basic operating modes of Match, Detect, Average, and Data. The Average mode is obtained when J, K and L are left open. The second pole of the rotary switch is used to select between two different Detect modes used in a software program developed for the second prototype.

Figure 1.18 shows the mechanical location of all major TDRM components within the chassis.

1.6 TDRM Hardware Problems

Several hardware problems emerged as the TDRM was built and tested. The first problem was noise on the TDR waveform which reduced accuracy initially to plus or minus 12 feet. The problem was solved by the appropriate application of filters and the separation of the computer power supply and sampling circuit power supply. Separate power supplies were used since the alternative would have been very large filter capacitors.

Occasionally the computer malfunctioned in an open air room temperature environment, a new computer chip improved performance but worked best with fan cooling. To insure reliable performance chip heat sinks should be used in field units on the CPU and PROM's to eliminate this problem. During actual testing an output buffer and a RAM eventually failed. Before failure these components operated intermittently causing

erroneous results at times. Only after replacement did the TDRM unit operate without incident. These two failures can be traced to infant mortality experienced with any solid state component. Burn-in can eliminate this problem.

Computer hardware problems point out the need for a good diagnostic program to check out microcomputers before they are used in an instrument. The program is also a necessity in troubleshooting defective microcomputers. The analog sampling circuitry poses no great problem in troubleshooting since it can be debugged using a logical building block approach.

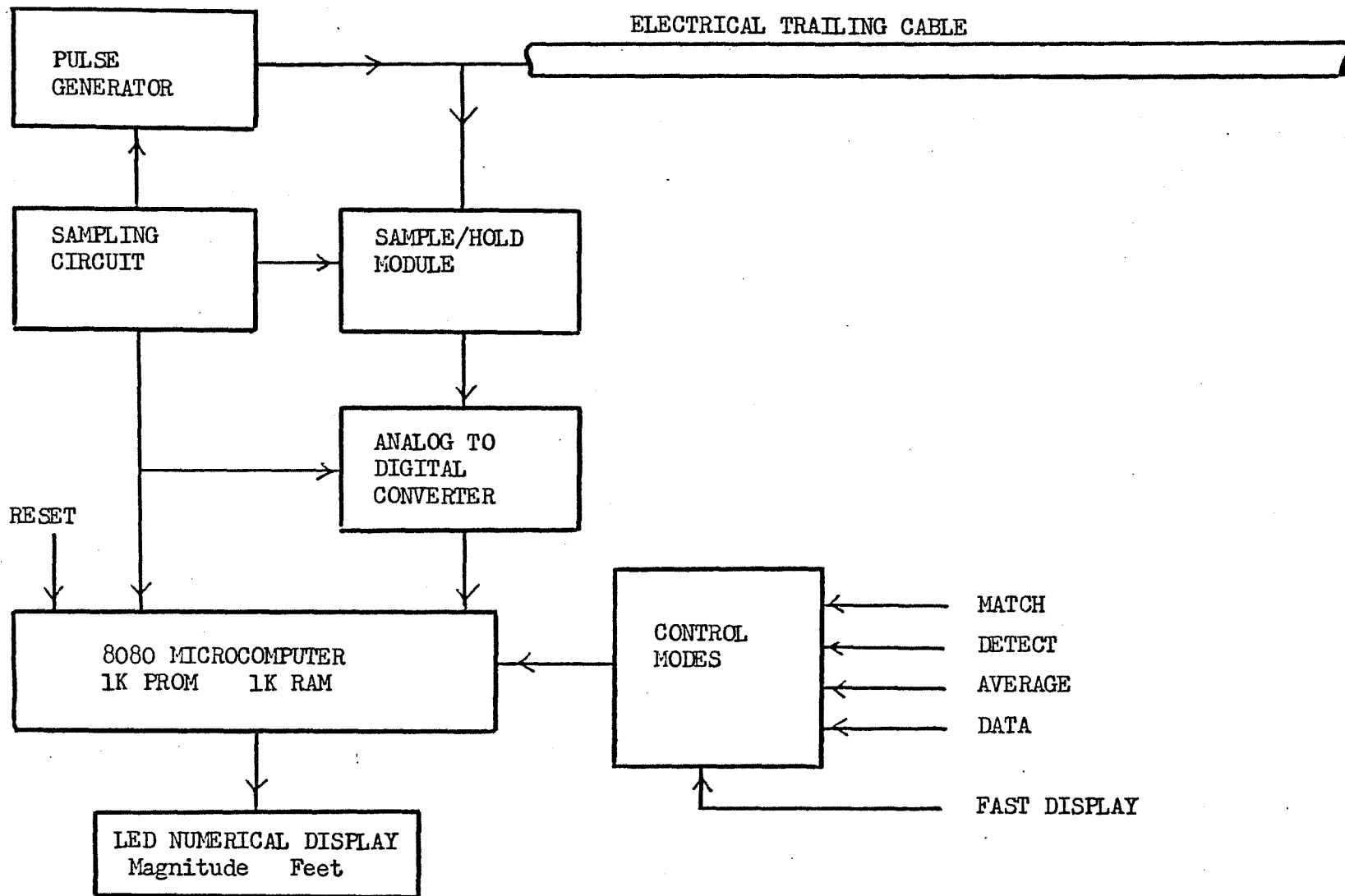


Fig. 1.1 Block Diagram of TDRM

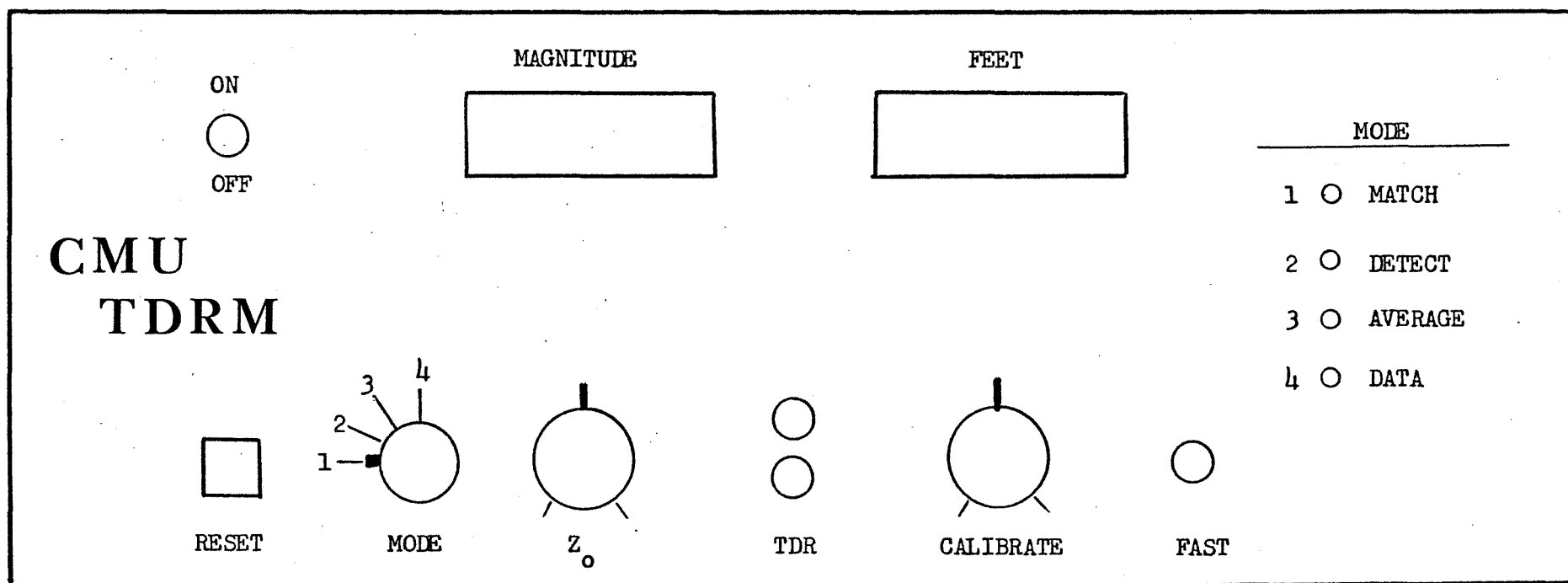


Fig. 1.2 TDRM Front Panel Prototype 1

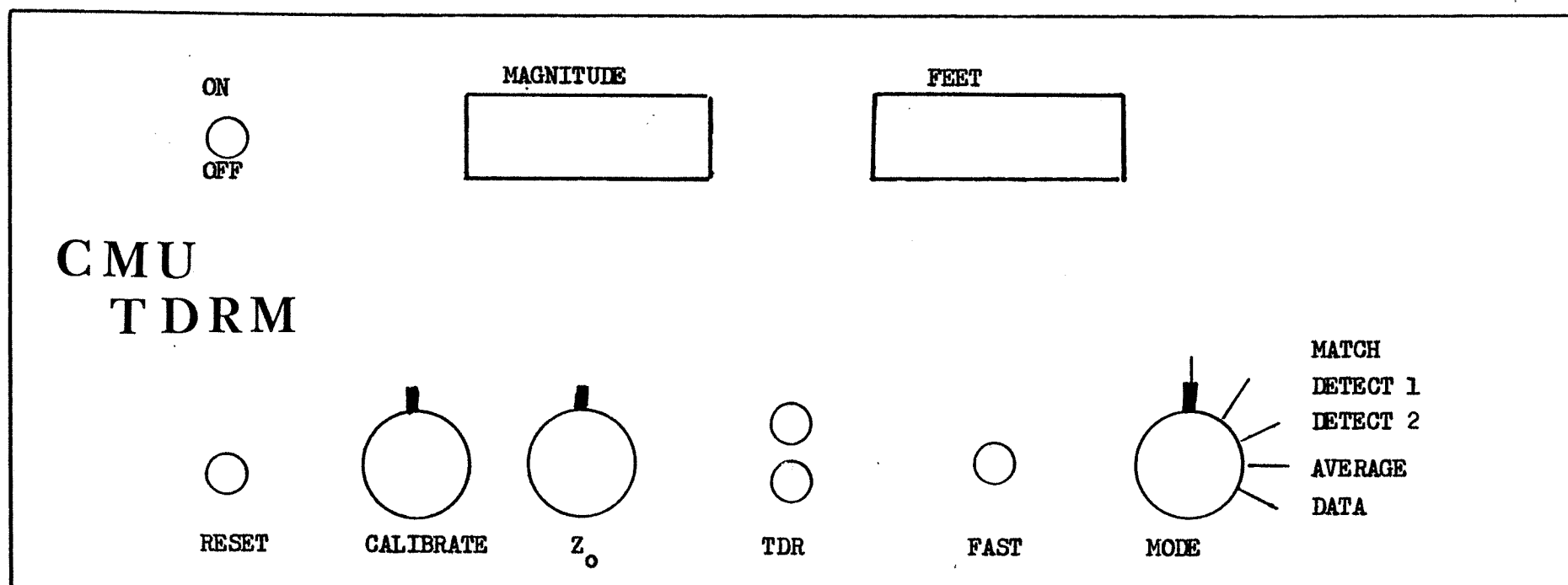
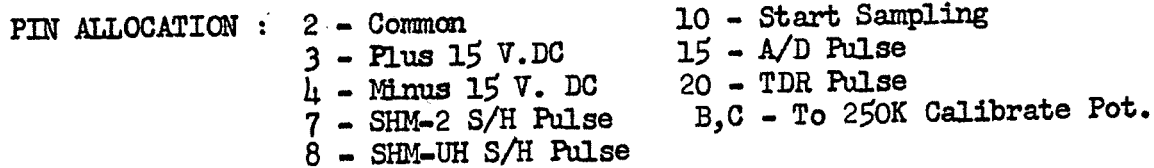


Fig. 1.3 Front Panel TDRM Prototype 2

Note: All resistors $\frac{1}{2}$ watt
All capacitors mylar
except * Electrolytic
Ceramic



-20-

SAMPLING AND TIMING DIAGRAM

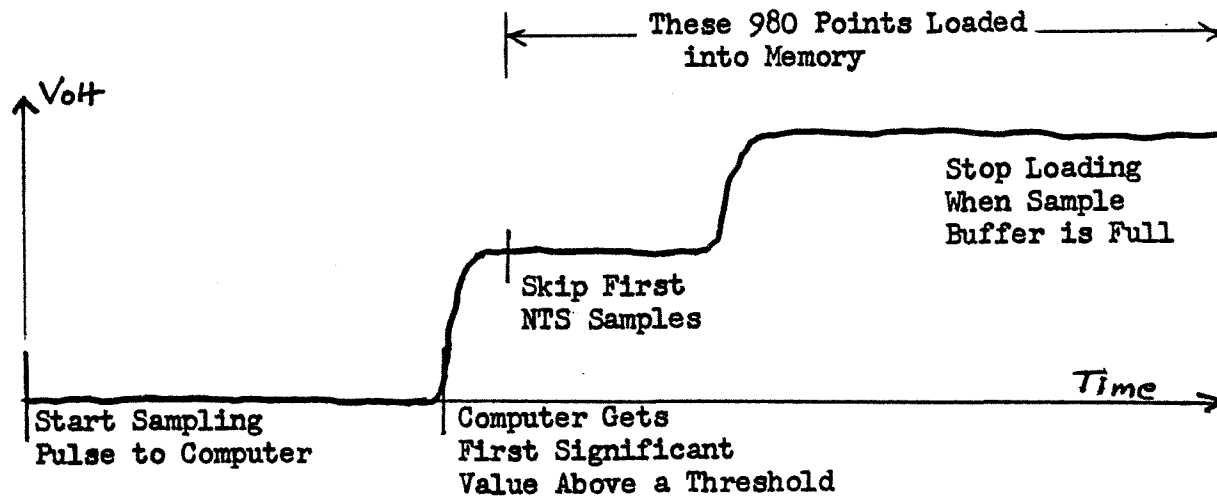
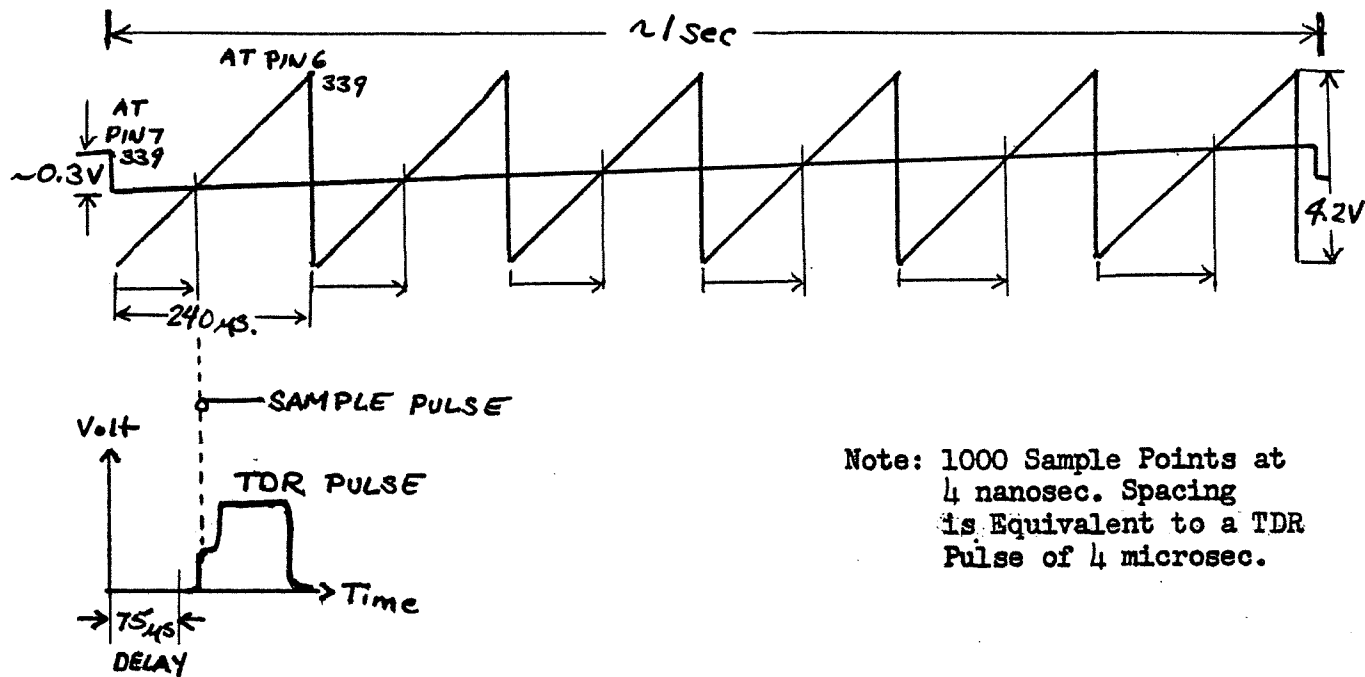
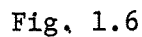


Fig. 1.5

SAMPLE/HOLD & ANALOG/DIGITAL CARD DIAGRAM



SECOND PROTOTYPE

SAMPLE/HOLD & ANALOG/DIGITAL CARD DIAGRAM

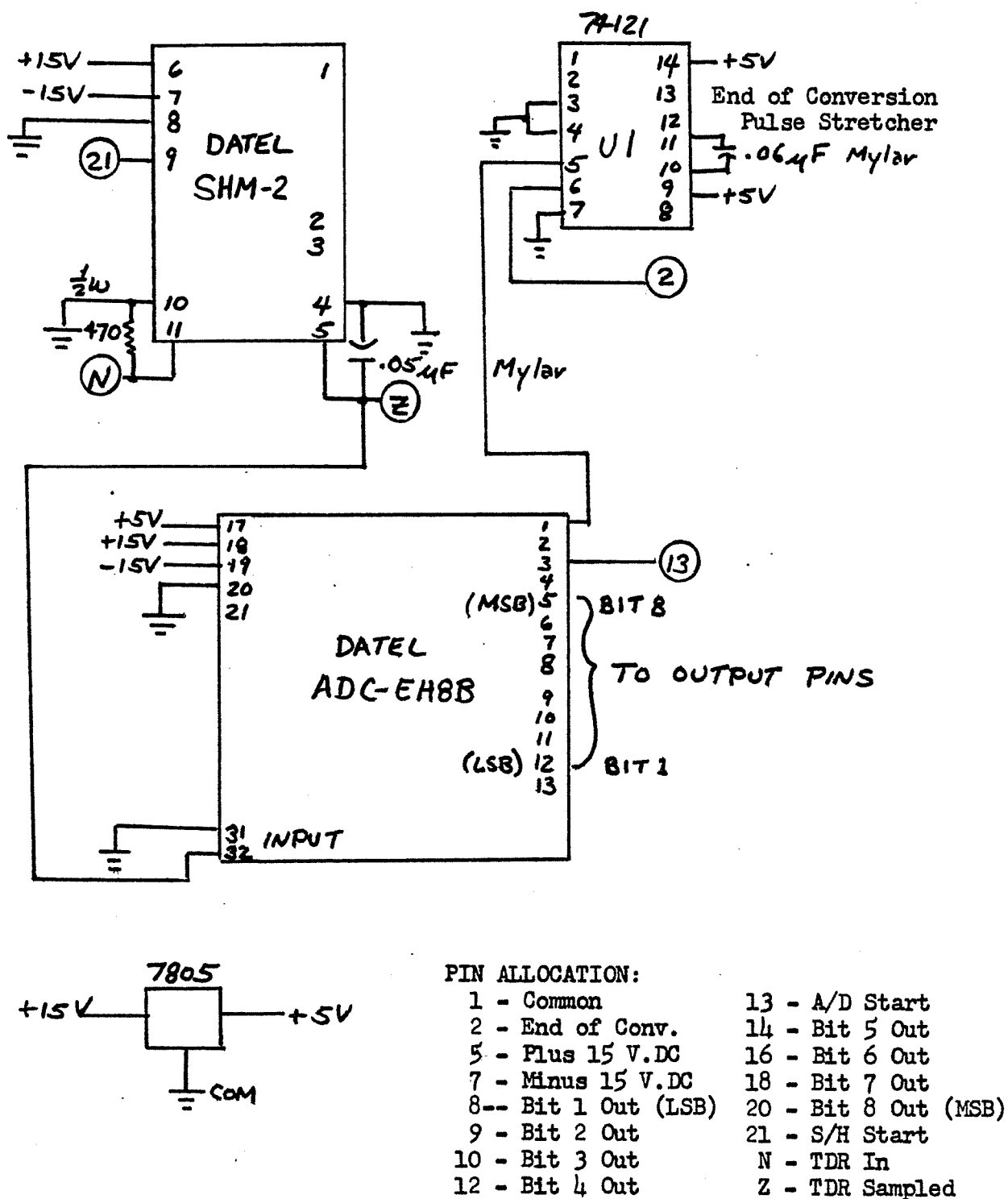
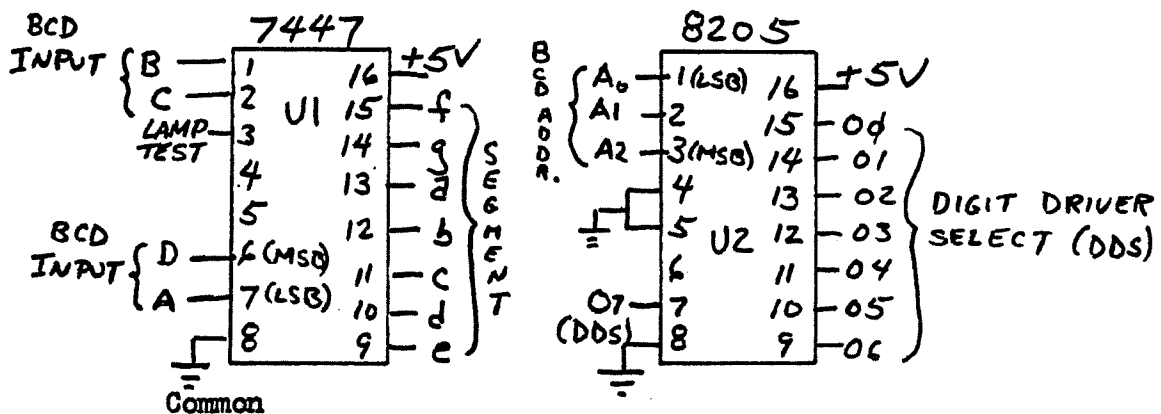
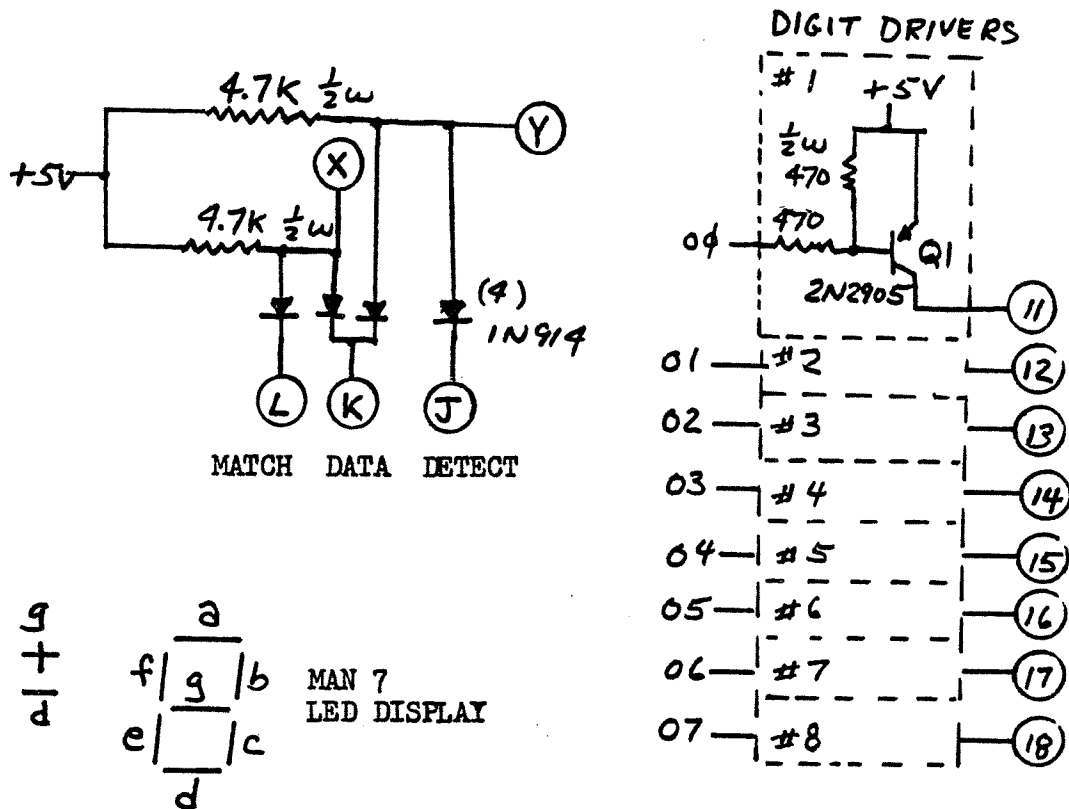


Fig. 1.7

OUTPUT DECODER-DRIVER CARD DIAGRAM



PIN ALLOCATION:		
A thru F - Segments	1 - BCD Input A	11 - Digit 1 Driver
a thru f	2 - BCD Input B	12 - Digit 2 Driver
H - Segment g	3 - BCD Input C	13 - Digit 3 Driver
L - MATCH	4 - BCD Input D	14 - Digit 4 Driver
K - DATA	5 - BCD Address A0	15 - Digit 5 Driver
J - DETECT	6 - BCD Address A1	16 - Digit 6 Driver
Y - Output #3, Bit 4	7 - BCD Address A2	17 - Digit 7 Driver
X - Output #3, Bit 1	9 - Lamp Test	18 - Digit 8 Driver
		21 - Plus 5 V.DC
		22 - Common

Fig. 1.8

From Digit Decoder/Driver Card Terminals
18 Thru 11 of Digit Drivers

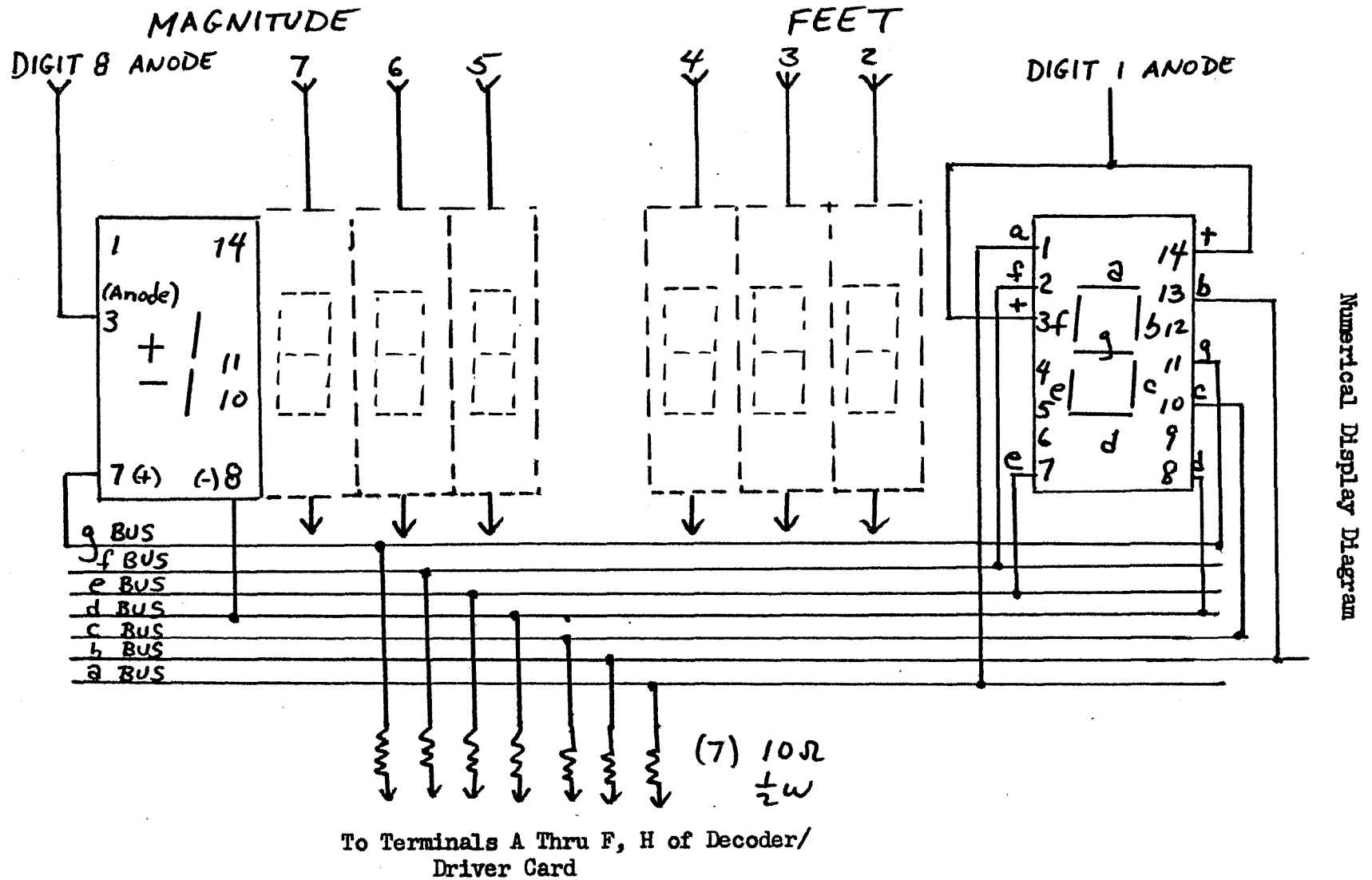


Fig. 1.9

PROLOG 8811 CPU

BLOCK DIAGRAM

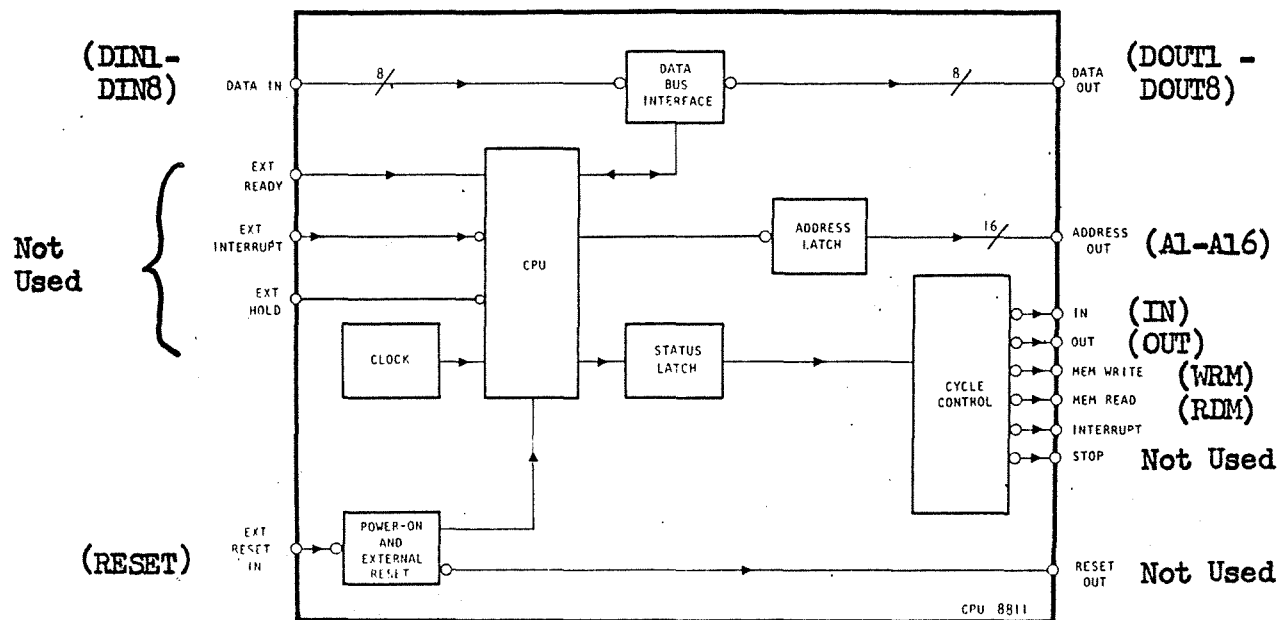


Fig. 1.10

PROLOG 8112 MEMORY

BLOCK DIAGRAM

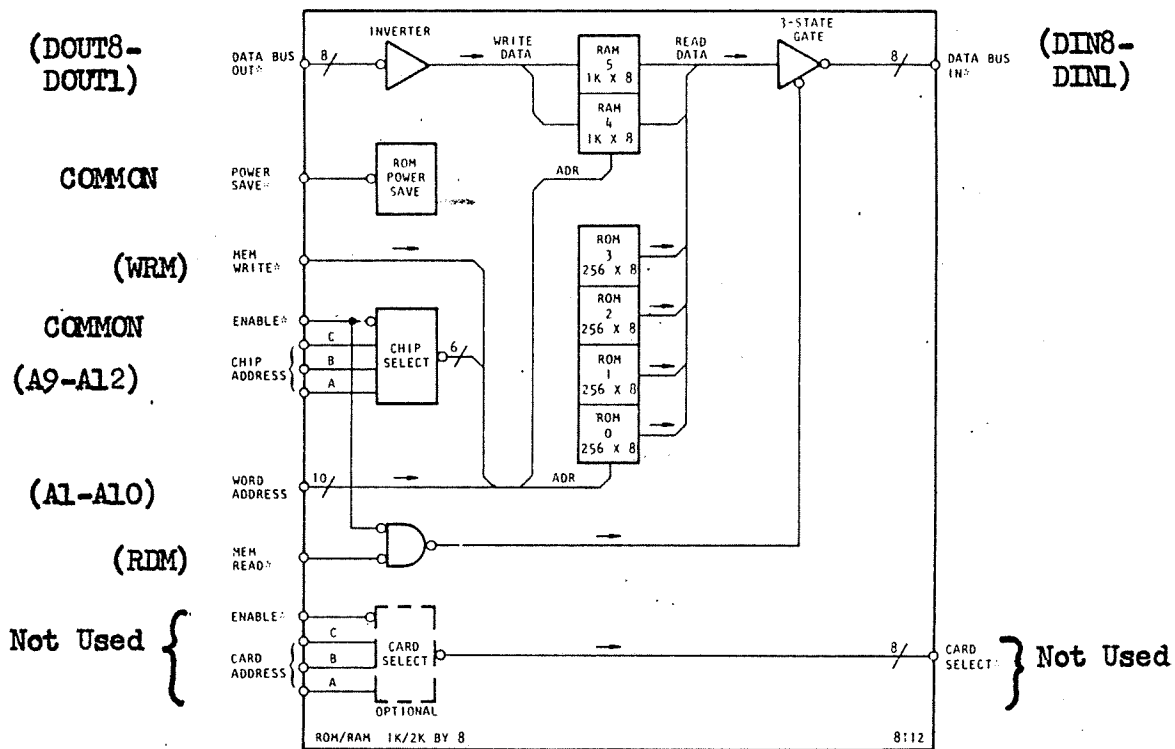


Fig. 1.11

PROLOG 8113 I/O

BLOCK DIAGRAM

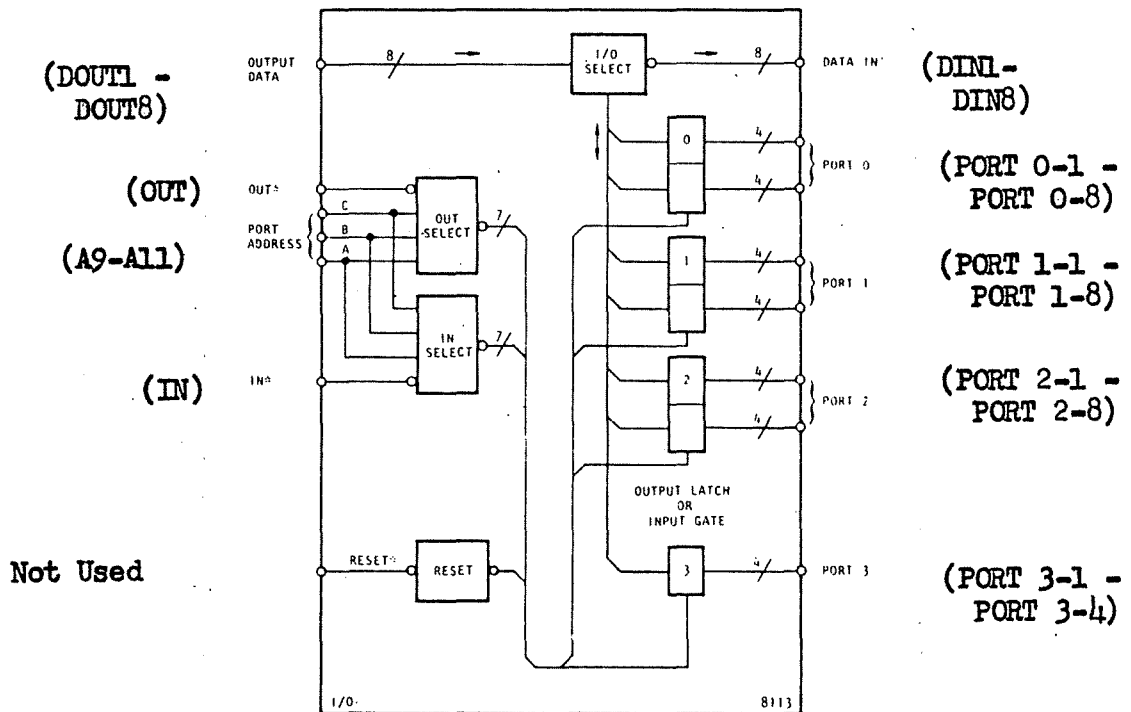


Fig. 1.12

PROLOG 8811 CPU
PRINTED CIRCUIT CARD PIN IDENTIFICATION

PLUS 5 V DC	2	1	PLUS 5 V DC
COMMON	4	3	COMMON
MINUS 10 V DC	6	5	MINUS 10 V DC
DIN8	8	7	DOUT8
DIN7	10	9	DOUT7
DIN6	12	11	DOUT6
DIN5	14	13	DOUT5
DIN4	16	15	DOUT4
DIN3	18	17	DOUT3
DIN2	20	19	DOUT2
DIN1	22	21	DOUT1
A16	24	23	A8
A15	26	25	A7
A14	28	27	A6
A13	30	29	A5
A12	32	31	A4
A11	34	33	A3
A10	36	35	A2
A9	38	37	A1
STOP	40	39	WAIT
IN	42	41	OUT
SPARE	44	43	WRM
RDM	46	45	INTR
HLTA	48	47	IREQ
HLD	50	49	RDY
RESET	52	51	TTL 1
SYNC	54	53	RST
PLUS 12 V DC	56	55	PLUS 12 V DC

Fig. 1.13

PROLOG 8112 MEMORY

PRINTED CIRCUIT CARD PIN IDENTIFICATION

PLUS 5 V DC	2	1	PLUS 5 V DC
COMMON	4	3	COMMON
MINUS 10 V DC	6	5	MINUS 10 V DC
DIN8	8	7	DOUT8
DIN7	10	9	DOUT7
DIN6	12	11	DOUT6
DIN5	14	13	DOUT5
DIN4	16	15	DOUT4
DIN3	18	17	DOUT3
DIN2	20	19	DOUT2
DIN1	22	21	DOUT1
N.C.	24	23	A8
N.C.	26	25	A7
N.C.	28	27	A6
A12	30	29	A5
A10	32	31	A4
A9	34	33	A3
A10	36	35	A2
A9	38	37	A1
N.C.	40	39	N.C.
N.C.	42	41	N.C.
N.C.	44	43	N.C.
N.C.	46	45	N.C.
A11	48	47	COMMON
COMMON	50	49	N.C.
A12	52	51	SPARE
RDM	54	53	SPARE
WRM	56	55	POWER SAVE- COMMON

*N.C. -
NOT CONNECTED

Fig. 1.14

PROLOG 8113 I/O

PRINTED CIRCUIT CARD PIN IDENTIFICATION

PLUS 5 V DC	2	1	PLUS 5 V DC
COMMON	4	3	COMMON
SPARE	6	5	SPARE
DIN8	8	7	PORT 2-8
DIN7	10	9	PORT 2-7
DIN6	12	11	PORT 2-6
DIN5	14	13	PORT 2-5
DIN4	16	15	PORT 2-4
DIN3	18	17	PORT 2-3
DIN2	20	19	PORT 2-2
DIN1	22	21	PORT 2-1
PORT 3-4	24	23	DOUT8
PORT 3-3	26	25	DOUT7
PORT 3-2	28	27	DOUT6
PORT 3-1	30	29	DOUT5
A9	32	31	DOUT4
A10	34	33	DOUT3
A11	36	35	DOUT2
OUT	38	37	DOUT1
IN	40	39	RST
PORT 0-8	42	41	PORT 1-8
PORT 0-7	44	43	PORT 1-7
PORT 0-6	46	45	PORT 1-6
PORT 0-5	48	47	PORT 1-5
PORT 0-4	50	49	PORT 1-4
PORT 0-3	52	51	PORT 1-3
PORT 0-2	54	53	PORT 1-2
PORT 0-1	56	55	PORT 1-1

Fig. 1.15

PROLOG MICROCOMPUTER I/O UTILIZATION

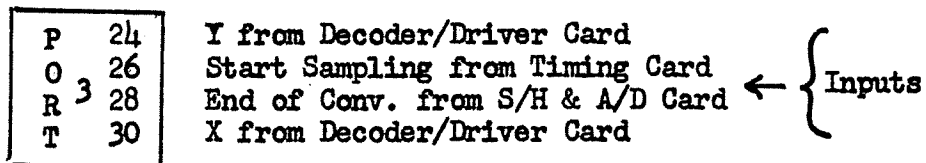
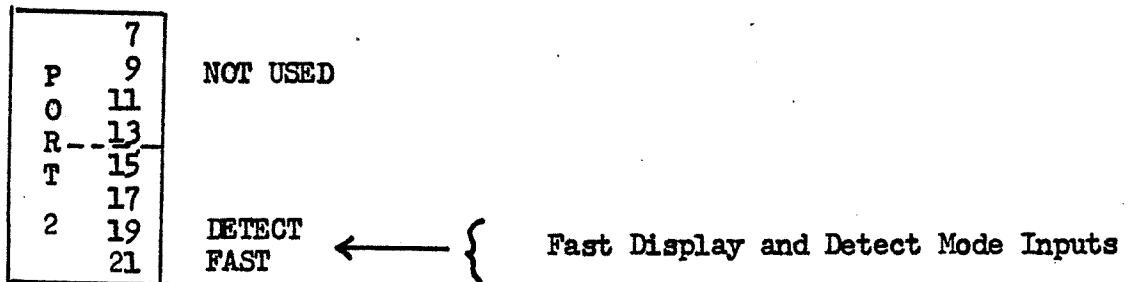
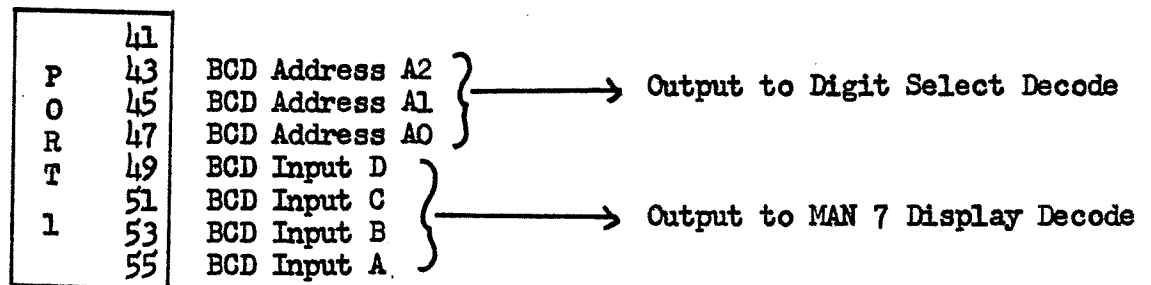
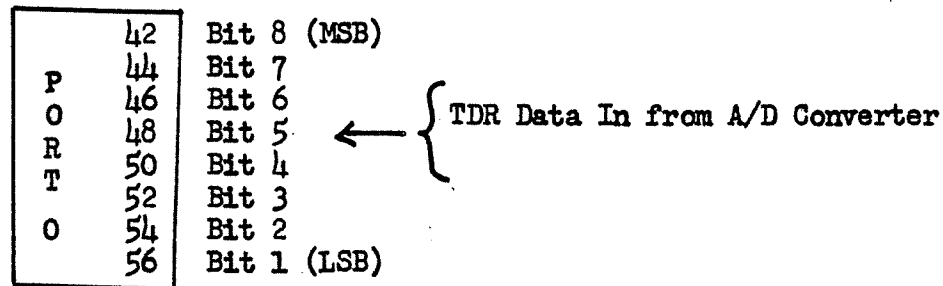
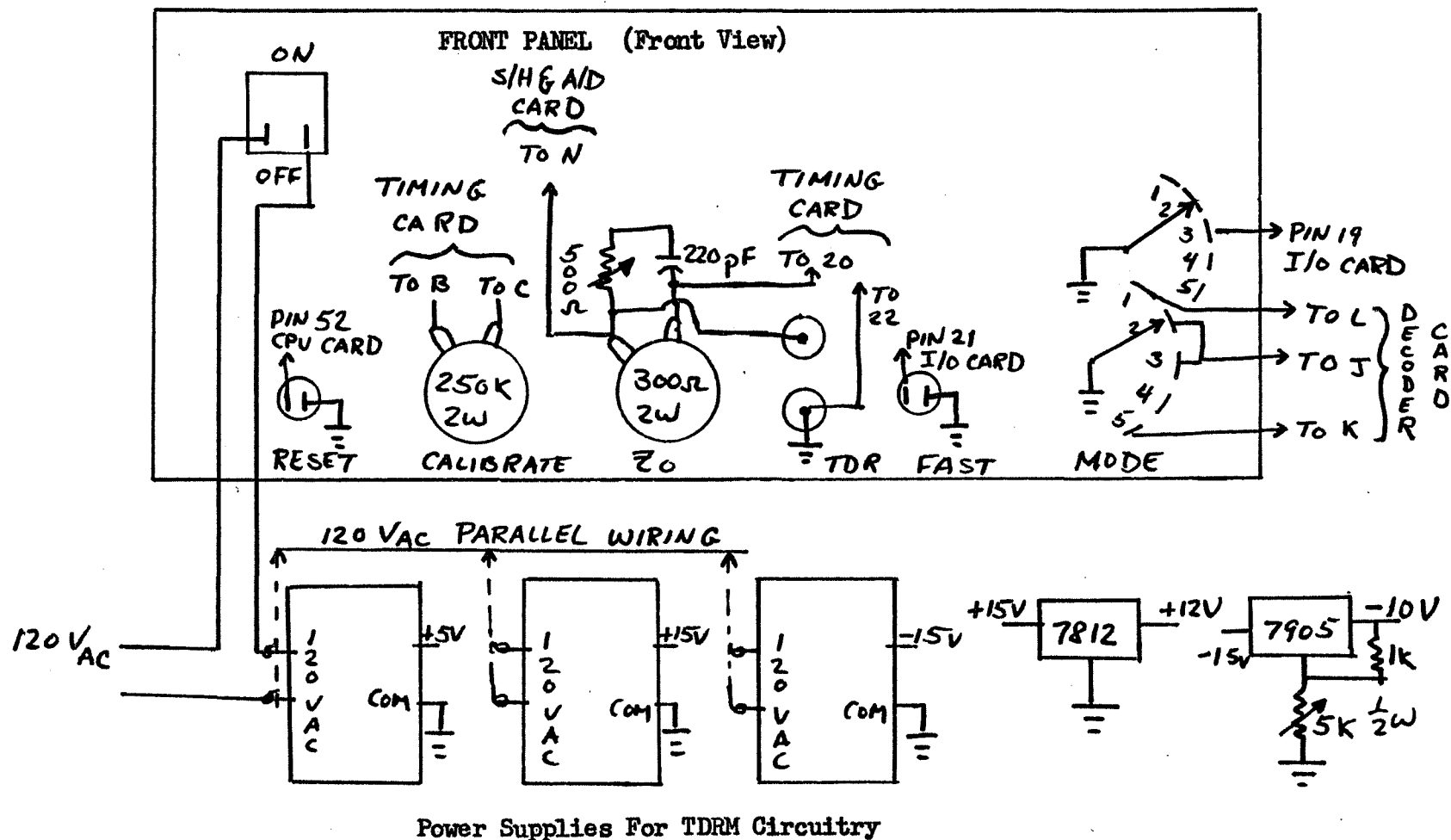


Fig. 1.16



FRONT PANEL AND POWER SUPPLY DIAGRAM

Fig. 1.17

LOCATION OF MAJOR COMPONENTS IN TDRM

(Top View)

-15 Volt DC Power Supply		PROLOG 8811 CPU	PROLOG 8112 Memory	PROLOG 8113 I/O	Output Decoder/Driver Card	Timing Card	Sample/Hold & A/D Card	(First Prototype Only) Location of Separate +5,+15 & -15 V DC Supply
								+15 Volt DC Power Supply
-10 Volt DC + 5 Volt DC Power Supplies								+5 Volt DC Power Supply

Fig. 1.18

Numerical LED Display Card

FRONT PANEL

Chapter 2

SOFTWARE

Several different algorithms were investigated for use with the TDRM unit. Best location accuracy can be obtained by the use of adjacent point comparison algorithms if the change of slope of the TDR waveform at the cable end point occurs over 25 or less sample points. On highly capacitive cables the cable end point change of slope may require 100 or more sample points. Thus, adjacent point comparisons are unable to distinguish between minor discontinuities and the cable end point.

To overcome this problem a comparison between sample points spaced a constant "X" points apart was used. The algorithm using this comparison technique gave good results for a wide variety of cables, but some inaccuracy in locating intermediate discontinuities was observed.

The first prototype uses the "X point comparison" algorithm for end point and intermediate discontinuity location. The second prototype uses the "X point comparison" algorithm for end point location and the adjacent point comparison for location of intermediate discontinuities. Because the "X point comparison" technique requires about 50 points to accurately detect the end point and ignore initial TDR waveform ringing, cable faults in less than 46 feet of cable cannot be located. The second prototype has a Detect 2 mode which permits the location of discontinuities for less than 50 feet. Such a mode is possible where adjacent comparison techniques are used for intermediate discontinuity location.

Because of TDR waveform noise, it was found that averaging several end points could reduce the variance in readings from ± 4 feet to ± 1 foot

for some types of cables.

This chapter describes the algorithms and software used in the TDRM. A computer printout of the program used in the second prototype is included.

2.1 The Algorithm

To insure compatibility with the microcomputer only simple algorithms were investigated to detect faults within the cable. If adjacent points in the sample buffer are subtracted from each other, the first difference computed is equivalent to taking the first derivative of the TDR waveform with respect to distance. This first derivative is used to detect discontinuities in the TDR waveform. If adjacent first difference points are subtracted from each other, the second difference is computed which is equivalent to taking the second derivative of the TDR waveform. The second derivative is used to detect changes in slope of the TDR waveform.

After investigating several algorithms using both first and second difference information, the following algorithm was chosen to be used in initial field tests. This algorithm will eventually be modified and optimized as a result of extensive field tests to be conducted with second generation prototypes.

Figure 2.1 shows a typical TDR waveform with a parallel resistive fault located somewhere within the cable. If the first difference of the TDR waveform is calculated, the waveform of Fig. 2.1b will result. Note that the end of the cable is detected by a major positive discontinuity in the first difference waveform; whereas, the resistive fault is detected by a small negative discontinuity. Initial tests with adjacent first differences revealed detection difficulties with highly capacitive cables

which gave slow rates of change of slope. To overcome this problem the first difference was calculated by taking the difference between the n and the $n + x$ sample point. Thus larger magnitudes were obtained for use by the detection routine. Since the TDR waveform has a finite slope at each discontinuity, x points on either side of the discontinuity are usually erased from memory to eliminate confusing discontinuity information. A discontinuity is said to occur at the first major change in slope of the first difference waveform. Thus the other first difference information in the near vicinity of this point is extraneous to the fault location routine.

If an arbitrary threshold is chosen, a scan of all first difference points will reveal all major faults above this threshold value. Since a search for the end point is made on the first scan, the first major fault should be the open end of the cable (or short end, if manually shorted). This first major discontinuity is used for cable calibration. If the threshold value is too high, it will be reduced by one for each subsequent scan until a first major discontinuity is found. This major discontinuity is usually interpreted to be the end of the cable in a non-faulted cable.

After the end point is determined, all discontinuities between this endpoint and the beginning of the cable are displayed in order of decreasing magnitude and increasing distance. The first prototype uses the same algorithm for both end point and intermediate discontinuity location. The second prototype uses the adjacent point comparison algorithm to find intermediate discontinuities. Exhaustive field tests will reveal which algorithm is preferred.

The major discontinuities and their locations should be manually

recorded and used for investigation with a probe type instrument before repair is effected. Since multiple discontinuities cause multiple reflections with confusing data, only major discontinuities should be first investigated and repair should always be effected on the first fault, since subsequent discontinuities may not be an indication of the existence of an actual fault. Thus optimum use of these algorithms or any TDR instrument requires the repair of the first discontinuity before subsequent ones can be accurately located. Of course small magnitude discontinuities can result from the temporary repair itself. With these considerations in mind, the algorithm can locate and detect a shunt fault of up to 500 ohms within the cable. Although higher values of resistance detection are possible, the random discontinuities of the average repaired trailing cable would appear as faults themselves. To eliminate this detection problem, a memory of the cable characteristics would have to be recorded on magnetic tape, and subsequently fed back into the TDRM for a before and after comparison. Such techniques have been successfully used with a mini-computer based instrument for highly accurate fault detection.

2.2 Software Program ^{3,4}

The TDRM software program was written in assembly language and converted to hexadecimal code for PROM programming through an assembler program. A general purpose assembler is written on a PDP-11/40 at CMU for use with the 8080 microprocessor. The Intellec 8 Mod 80 development unit also possesses an assembler for use in programming conversion of the mnemonics to hexadecimal code.

Each subroutine was debugged on the Intellec 8 Mod 80 development unit and a simulation tape combining the subroutines together was also

tested. The development unit speeds up the writing, testing and debugging of a microprocessor program. The main advantage of the development unit is that the program is both hardware and software debugged at the same time.

The basic flow diagram of the computer program is shown in Fig. 2.2. Note that the Average mode sums up the first major discontinuity detected by the Detect Program for eight separate sampled TDR waveforms and then performs a division by eight on the sum before displaying the average of the eight samples. This averaging processes may be extended to second, third, etc., discontinuities if necessary. Also eight entire waveforms can also be averaged before the first differences are calculated; however, extra memory, changes in hardware and longer calculation times are required for this approach.

The flow diagram of the Detect Program is shown in Figure 2.3. The procedure of the program is;

- (a) compute the first difference of the TDR waveform using point n and point $n + x$,
- (b) scan the first difference data for an absolute magnitude greater than a given threshold,
- (c) set the first detected point above this threshold as the endpoint,
- (d) if an endpoint is not found reduce the threshold until found,
- (e) erase x points on either side of the detected point,
- (f) reduce threshold to locate other discontinuities above a given minimum threshold,

- (g) erase x points on either side of these discontinuities,
- (h) display all discontinuities in decreasing order of magnitude and increasing distance.

For the second prototype the end point is found by setting x to 20 and intermediate points are found by setting x to 1.

The computer printout for the second TDRM prototype is annotated to aid in describing program flow.

The Main Program performs the required initializations and loads the digitized TDR samples into memory. It also decodes the mode control switch inputs to select the program mode. In the Detect Mode the Main Program displays all intermediate faults.

The Detect program consists of the end of the Main Program, the REC subroutine and the COMP subroutine. The REC subroutine finds the endpoint using the x point comparison technique and stores the location magnitude and sign in LDATA, MAGPT and SIGN RAM locations. The remaining discontinuities are determined by subtracting adjacent sample points between the beginning of the sample buffer and the LDATA point. The endpoint location and magnitude are displayed before using COMP to display all intermediate first difference points as computed by REC. DETECT 1 and DETECT 2 are selected in COMP as different starting addresses for intermediate discontinuity display.

The Average program is the front end of the REC program and does not use the COMP subroutine. Eight sets of TDR waveforms are analyzed. From each set of TDR waveforms the endpoint or major fault location and its respective magnitude are summed and stored. After eight such additions the DIV8 routine performs a division by 8 and the averaged first discontinuity location and magnitude is displayed.

The Match program displays the digitized value of a sample 16 points from the beginning of the TDR waveform. The Z_0 control is used to set the value stored in this 16th location to approximately 100. This process accomplishes impedance matching of the TDRM to the cable.

The Data program displays the decimal value from 0 to 255 of all data entered into the sample buffer. This program is used for troubleshooting and detail study of discontinuity data.

The receiving subroutines are supporting functions to the four major modes of operation. The Decode subroutine converts a binary number into 4 decimal digits for use with the display.

The Display subroutine blanks leading zeros and displays the BCD encoded digits in memory locations, SIGN M100, M10, M1, THOU, HUND, TENS and ONES.

The DIV8 is a simple division by 8 program for use with averaging programs.

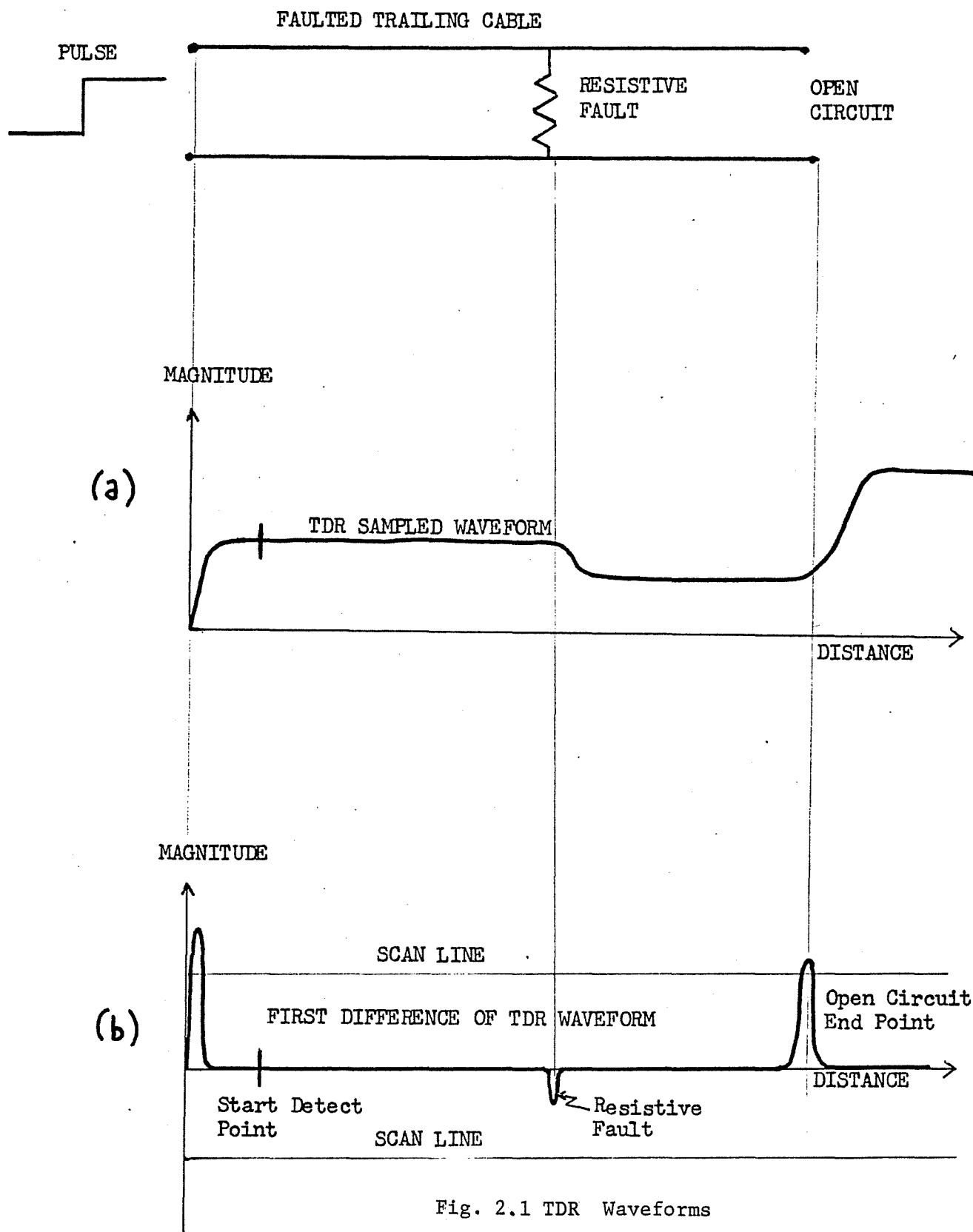


Fig. 2.1 TDR Waveforms

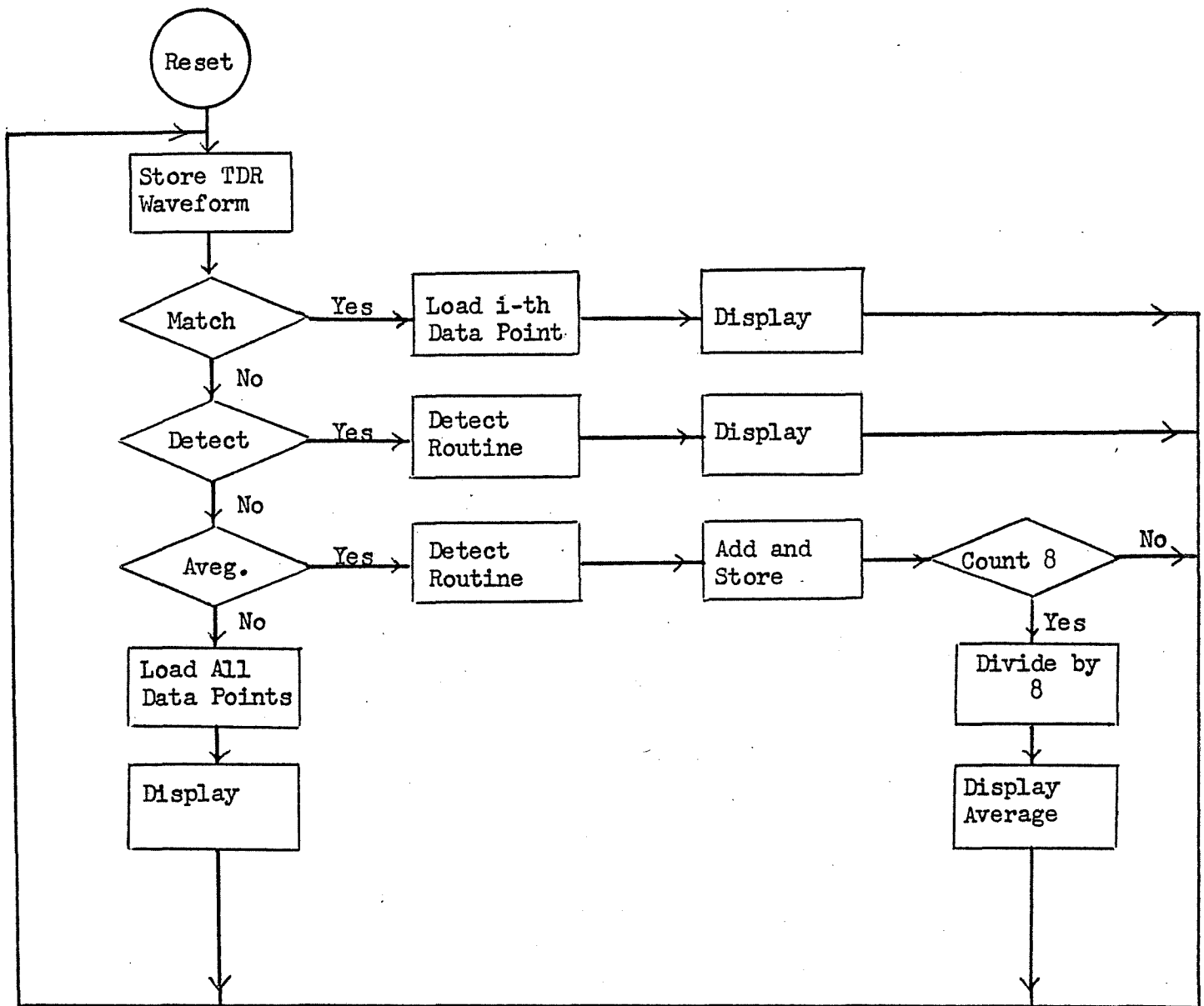


Fig. 2.2 TDRM Software Flow Chart

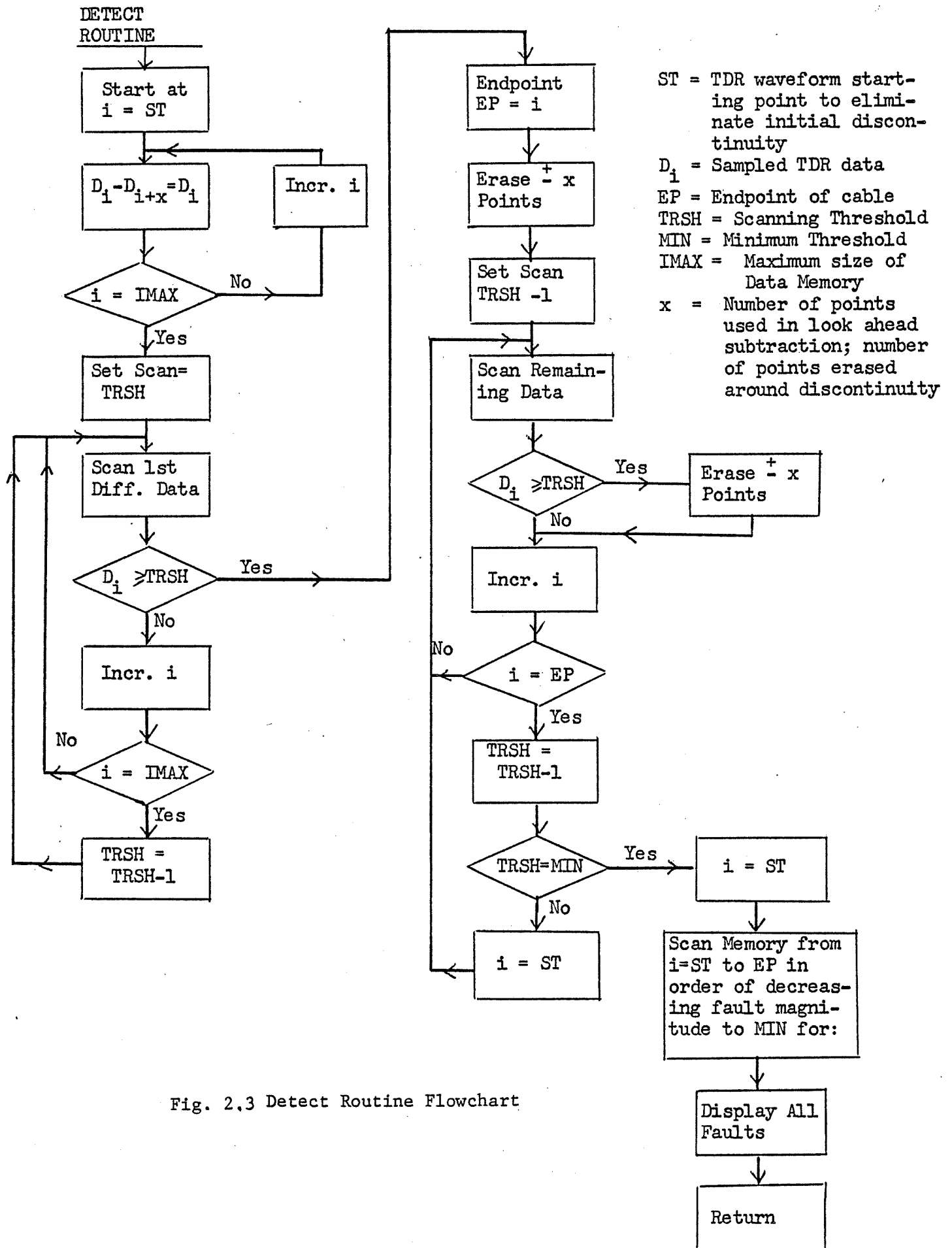


Fig. 2.3 Detect Routine Flowchart

TDRM PROGRAM
INTEL 8080 LANGUAGE

```

0812      SIGN EQU 812H
0813      M100 EQU 813H
0814      M10 EQU 814H
0815      M1 EQU 815H
0816      THOU EQU 816H
0817      HUND EQU 817H
0818      TENS EQU 818H
0819      ONES EQU 819H
0820      MAGPT EQU 820H
0821      ST01 EQU 821H
0822      ST02 EQU 822H
0823      ST03 EQU 823H
0824      ST04 EQU 824H
0810      LDATA EQU 810H
0100      DECODE EQU 100H
0155      DISPLA EQU 155H
0290      REC EQU 290H
0350      AVG EQU 350H
03F0      OTH EQU 3F0H
0200      MATCH EQU 200H
0232      DATA EQU 232H
0000      ORG 00H

```

MAIN PROGRAM

```

0000 C3E400      SAMP: JMP 0E4H

```

Initialize RAM

```

00E4 210000      LXI H,00H
00E7 222108      SHLD 821H
00EA 222308      SHLD 823H
00FD 3E07        MVI A,07H
00EF 321308      STA 813H

```

Reset Count for Average Program

```

00F2 3E8F        MVI A,8FH
00F4 D301        OUT 1H
00F6 C30300      JMP 03H

```

Blank Last Digit

```

0003 211008      LXI H,810H
0006 F9          SPHL
0007 212508      LXI H,825H
000A DB03        WAIT: IN 3H
000C 00          NOP

```

Reset Stack

Get Address of Data Area
Sampling Started?

```

000D E602        ANI 2H
000F CA0A00      JZ WAIT
0012 DB03        HOLD1: IN 3H
0014 00          NOP
0015 E604        ANI 4H
0017 CA1200      JZ HOLD1
001A DB00        HOLD0: IN 0H
001C FE38        CPI 38H
001E FA1200      JM HOLD1

```

No

Yes, Get First Meaningful Sample

```

0021 110000      LXI D,00H
0024 14          SKIP: INR D
0025 15          DCR D
0026 C22E00      JNZ SKIP1
0029 1C          INR E
002A 1D          DCR E
002B CA4200      JZ H1

```

SLT- Start Load Tolerance
First Meaningful Sample is Read
NTS- Number of Points to Skip
0?

No

Maybe
Yes

002E	DB03	SKIP1: IN 3H
0030	00	NOP
0031	E604	ANI 4H
0033	CA2E00	JZ SKIP1
0036	DB03	SKIP0: IN 3H
0038	00	NOP
0039	E604	ANI 4H
003B	C23600	JNZ SKIP0
003E	1B	DCX D
003F	C32400	JMP SKIP
0042	DB03	H1: IN 3H
0044	00	NOP
0045	E604	ANI 4H
0047	CA4200	JZ H1
004A	DB00	H0: IN 00H
004C	77	MOV M, A
004D	3EFF	MVI A, 0FFH
004F	BD	CMP L
0050	C25900	JNZ NOTYT
0053	3E0B	MVI A, 0BH
0055	BC	CMP H
0056	CA5D00	JZ PROSS
0059	23	NOTYT: INX H
005A	C34200	JMP H1
005D	DB03	PROSS: IN 3H
005F	E609	ANI 9H
0061	FE01	CPI 1H
0063	CA0002	JZ MATCH
0066	FE08	CPI 8H
0068	CA3202	JZ DATA
006B	FE09	CPI 9H
006D	CA5003	JZ AVG
0070	CD9002	CALL REC
0073	1E06	MVI E, 6H
0075	D5	LOOP: PUSH D
0076	CD8A00	CALL COMP
0079	7A	MOV A, D
007A	2F	CMA
007B	3C	INR A
007C	57	MOV D, A
007D	CD8A00	CALL COMP
0080	D1	POP D
0081	15	DCR D
0082	7A	MOV A, D
0083	BB	CMP E
0084	C27500	JNZ LOOP
0087	C30000	JMP SAMP

No, Skip Data

Load Up Sample Buffer

Buffer Full?

No
Maybe
Yes

No

Matching Mode?

Yes
Data Mode?
Yes
Average Mode?
Yes
Detect Mode
MST- Minimum Scan Tolerance
Save Plus Mag. D
Display All Faults of Mag. D
Negate D

Display All Faults of Mag. -D
Restore Plus D
Decrement Magnitude
Minimum Scan Tolerance?

No
Yes

This subroutine scans the data points for a specific value of magnitude passed in register D, and displays all occurrences of this magnitude.

```

008A C3EC03  COMP: JMP 3ECH
03EC 214C08  LXI H,84CH
03EF DB02    IN 02H
03F1 E602    ANI 02H
03F3 C28D00  JNZ 08DH
03F6 212608  LXI H,826H
03F9 C38D00  JMP 08DH
008D 7E      DOSMP: MOV A,M
008E BA      CMP D
008F C2D100  JNZ NOTEQ
0092 A7      ANA A
0093 FA9F00  JM MAGN
0096 3E79    MVI A,79H
0098 321208  STA SIGN
009B 4A      MOV C,D
009C C3A800  JMP BACK
009F 3E70    MAGN: MVI A,70H
00A1 321208  STA SIGN
00A4 7A      MOV A,D
00A5 2F      CMA
00A6 3C      INR A
00A7 4F      MOV C,A
00A8 0600    BACK: MVI B,00H
00AA CD0001  CALL DECODE
00AD 3A1908  LDA ONES
00B0 321508  STA M1
00B3 3A1808  LDA TENS
00B6 321408  STA M10
00B9 3A1708  LDA HUND
00BC 321308  STA M100
00BF E5      PUSH H
00C0 01DBF7  LXI B,0F7DBH
00C3 09      DAD B
00C4 010000  LXI B,00H
00C7 09      DAD B
00C8 44      MOV B,H
00C9 4D      MOV C,L
00CA E1      POP H
00CB CD0001  CALL DECODE
00CE CD5501  CALL DISPLA
00D1 3A1008  NOTEQ: LDA LDATA
00D4 BD      CMP L
00D5 C2DF00  JNZ INDEX
00D8 3A1108  LDA LDATA+1
00DB BC      CMP H
00DC CAE300  JZ OUTA
00DF 23      INDEX: INX H
00E0 C38D00  JMP DOSMP
00E3 C9      OUTA: RET

```

Get Address of First Data Point
Detect 1?

Yes
No, Detect 2 -- New Address

Current Point Equal Magnitude?

No
Yes, Magnitude Negative?
Yes
No, Output a PLUS

Pass Magnitude to Decode
Output a MINUS

Pass Magnitude to Decode

Decode Magnitude Digits
Store in Output Buffers

Save Point Address
Compute Point Number in Feet

Restore Point Address
Pass FEET to Decode
Display Magnitude and Feet
All Points Done?

No

Yes
No
Do Rest

This subroutine will decode the binary number (positive) passed to it in B and C registers into 4 decimal digits ready for output. THOU, HUND, TENS, ONES.

```

0100 ES      DECODE: PUSH H
0101 D5      PUSH D
0102 69      MOV L,C
0103 60      MOV H,B
0104 97      SUB A
0105 1118FC  LXI D,-1000
0108 19      D1000: DAD D
0109 24      INR H
010A 25      DCR H
010B FA1201  JM OUT1
010E 3C      INR A
010F C30801  JMP D1000
0112 11E803  OUT1: LXI D,1000
0115 19      DAD D
0116 F630    ORI 30H
0118 321608  STA THOU
011B 97      SUB A
011C 119CFF  LXI D,-100
011F 19      D100: DAD D
0120 24      INR H
0121 25      DCR H
0122 FA2901  JM OUT2
0125 3C      INR A
0126 C31F01  JMP D100
0129 116400  OUT2: LXI D,100
012C 19      DAD D
012D F620    ORI 20H
012F 321708  STA HUND
0132 97      SUB A
0133 11F6FF  LXI D,-10
0136 19      D10: DAD D
0137 24      INR H
0138 25      DCR H
0139 FA4001  JM OUT3
013C 3C      INR A
013D C33601  JMP D10
0140 110A00  OUT3: LXI D,10
0143 19      DAD D
0144 F610    ORI 10H
0146 321808  STA TENS
0149 7D      MOV A,L
014A F600    ORI 00H
014C 321908  STA ONES
014F D1      POP D
0150 E1      POP H
0151 C9      RET
0152 00      NOP
0153 00      NOP
0154 00      NOP

```

This subroutine displays the output buffer, blanking leading zero digits.

0155	E5	DISPLA: PUSH H	
0156	3A1308	LDA M100	
0159	E60F	ANI 0FH	M100 equal 0?
015B	CA6301	JZ BL1	Blank It
015E	F660	ORI 60H	No, Fix Code
0160	C3F801	JMP 1F8H	
01F8	321308	STA 813H	
01FB	C3F900	JMP 0F9H	
00F9	3A1408	LDA M10	
00FC	C37001	JMP 170H	
0163	3E8F	BL1: MVI A,8FH	Blank M100
0165	321308	ST1: STA M100	
0168	3A1408	LDA M10	
016B	E60F	ANI 0FH	M10 equal 0?
016D	CA7501	JZ BL2	Blank It
0170	F650	ORI 50H	No, Fix Code
0172	C37701	JMP ST2	
0175	3E8F	BL2: MVI A,8FH	Blank M10
0177	321408	ST2: STA M10	
017A	3A1508	LDA M1	
017D	E60F	ANI 0FH	
017F	F640	ORI 40H	Fix Code for M1
0181	321508	STA M1	
0184	3A1608	LDA THOU	
0187	E60F	ANI 0FH	Blank Thou?
0189	C2AB01	JNZ OUTIT	No
018C	3E8F	MVI A,8FH	
018E	321608	STA THOU	
0191	3A1708	LDA HUND	Blank Hund?
0194	E60F	ANI 0FH	
0196	C2AB01	JNZ OUTIT	No
0199	3E8F	MVI A,8FH	
019B	321708	STA HUND	
019E	3A1808	LDA TENS	Blank Tens?
01A1	E60F	ANI 0FH	
01A3	C2AB01	JNZ OUTIT	No
01A6	3E8F	MVI A,8FH	
01A8	321808	STA TENS	
01AB	210020	OUTIT: LXI H,2000H	Load Display Time Counter
01AE	DB02	IN 02H	
01B0	E601	ANI 01H	Fast Display?
01B2	C2B801	JNZ DLOOP	No
01B5	210001	LXI H,100H	Yes, Reload Display Time Counter
01E8	3A1208	DLOOP: LDA SIGN	Output
01BB	00	NOP	
01BC	D301	OUT 1H	
01BE	3A1308	LDA M100	
01C1	00	NOP	
01C2	D301	OUT 1H	
01C4	3A1408	LDA M10	
01C7	00	NOP	
01C8	D301	OUT 1H	
01CA	3A1508	LDA M1	
01CD	00	NOP	
01CE	D301	OUT 1H	

01D0	3A1608	LDA THOU
01D3	00	NOP
01D4	D301	OUT 1H
01D6	3A1708	LDA HUND
01D9	00	NOP
01DA	D301	OUT 1H
01DC	3A1808	LDA TENS
01DF	00	NOP
01E0	D301	OUT 1H
01E2	3A1908	LDA ONES
01E5	00	NOP
01E6	D301	OUT 1H
01E8	3E8F	MVI A,8FH
01EA	D301	OUT 1H
01EC	97	SUB A
01ED	2B	DCX H
01EE	B5	ORA L
01EF	C2B801	JNZ DLOOP
01F2	B4	ORA H
01F3	C2B801	JNZ DLOOP
01F6	E1	POP H
01F7	C9	RET

The MATCH Routine displays the digitized value of the waveform at MSNA (Matching Sample Number Address) for use with the Z₀ Potentiometer.

The DATA routine displays all samples stored in the sample buffer.

0200 0600	MATCH: MVI B, 0H	Get Matching Sample
0202 3A3508	LDA 835H	MSNA
0205 4F	MOV C, A	
0206 CD0001	CALL DECODE	Decode Binary to Decimal Digits
0209 3A1908	LDA ONES	
020C 321508	STA M1	
020F 3A1808	LDA TENS	
0212 321408	STA M10	
0215 3A1708	LDA HUND	
0218 321308	STA M100	
021B 3E8F	MVI A, 8FH	Blanking Number
021D 321208	STA SIGN	
0220 321608	STA THOU	
0223 321708	STA HUND	
0226 321808	STA TENS	
0229 321908	STA ONES	
022C CD5501	CALL DISPLA	Display Value at MSNA
022F C30000	JMP 00H	
0232 3E8F	DATA: MVI A, 8FH	Blank Sign
0234 321208	STA SIGN	
0237 110100	LXI D, 1H	Initial Data Point
023A 212508	LXI H, 825H	Start of Data
023D 0600	EACHP: MVI B, 0H	Pass Data Count
023F 4E	MOV C, M	
0240 CD0001	CALL DECODE	Decode
0243 3A1908	LDA ONES	Store in Magnitude Digits
0246 321508	STA M1	
0249 3A1808	LDA TENS	
024C 321408	STA M10	
024F 3A1708	LDA HUND	
0252 321308	STA M100	
0255 42	MOV B, D	Load Feet
0256 4B	MOV C, E	
0257 CD0001	CALL DECODE	Decode
025A CD5501	CALL DISPLA	Display Magnitude and Feet
025D 13	INX D	Increment Count
025E 23	INX H	Increment Data Address
025F 3E00	MVI A, 0H	All Points Done?
0261 BD	CMP L	Compare to last address plus 1
0262 C23D02	JNZ EACHP	
0265 3E0C	MVI A, 0CH	
0267 BC	CMP H	
0268 C23D02	JNZ EACHP	No
026B C30000	JMP 0000H	Yes

This subroutine is used with the Average Routine to perform a division by 8.

0271	AF	DIV8: XRA A
0272	7C	MOV A,H
0273	0F	RRC
0274	0F	RRC
0275	0F	RRC
0276	00	NOP
0277	67	MOV H,A
0278	AF	XRA A
0279	7D	MOV A,L
027A	0F	RRC
027B	0F	RRC
027C	0F	RRC
027D	E61F	ANI 1FH
027F	6F	MOV L,A
0280	7C	MOV A,H
0281	E6E0	ANI 0E0H
0283	B5	ORA L
0284	6F	MOV L,A
0285	7C	MOV A,H
0286	E61F	ANI 1FH
0288	67	MOV H,A
0289	C9	RET

This routine finds the cable end point and displays intermediate discontinuities above a tolerance level.

```

0290 0614      REC: MVI B,14H
0292 214908    DE1: LXI H,849H
0295 115708    LXI D,857H
0298 0E79      DE2: MVI C,79H
029A 1A        LDAX D
029B 96        SUB M
029C 322108    STA ST01
029F B7        ORA A
02A0 F2A702    JP PLUS
02A3 2F        CMA
02A4 3C        INR A
02A5 0E70      MVI C,70H
02A7 B8        PLUS: CMP E
02A8 FA8A02    JM 28AH
028A 13        INX D
028E C3BE02    JMP NOTY
02AB EB        XCHG
02AC 221008    SHLD LDATA
02AF 322008    STA MAGPT
02B2 79        MOV A,C
02B3 321208    STA SIGN
02B6 23        INX H
02B7 23        INX H
02B8 222208    SHLD ST02
02BB C3CF02    JMP EXIT
02BE 23        NOTY: INX H
02BF 7D        MOV A,L
02C0 FEDC      CPI 0DCH
02C2 C29802    JNZ DE2
02C5 7C        MOV A,H
02C6 FE0B      CPI 0BH
02C8 C29802    JNZ DE2
02CB 05        DCR B
02CC C39202    JMP DE1
02CF 212508    EXIT: LXI H,825H
02D2 23        DI: INX H
02D3 7E        MOV A,M
02D4 2B        DCX H
02D5 96        SUB M
02D6 77        MOV M,A
02D7 23        INX H
02D8 3A2208    LDA 822H
02DB BD        CMP L
02DC C2D202    JNZ D1
02DF 3A2308    LDA 823H
02E2 BC        CMP H
02E3 C2D202    JNZ D1

```

End Point Tolerance

Address of First Data Point

Address of Second Data Point

Load C register with Plus Sign

Load D register Data

Subtract M register Data

Magnitude Positive?

No, Negative

Load C register with Minus Sign

Compare with End Point Tolerance

Yes

No

Exchange D-E and H-L Registers

Store End Point Found in H-L

Store Magnitude

Store Sign of Magnitude

Store Endpoint for Next Routine EXIT

End of Data Buffer?

No

No

Yes, Decrement End Point Tolerance

Address of First Data Point

Subtract Adjacent Points

Store First Difference

End of Data to be Subtracted?

No

No

02E6	3A2008	LDA MAGPT
02E9	57	MOV D, A
02EA	2A1008	LHLD LDATA
02ED	4A	MOV C, D
02FE	CDA800	CALL BACK
02F1	2A1008	LHLD LDATA
02F4	2B	DCX H
02F5	2B	DCX H
02F6	2B	DCX H
02F7	2B	DCX H
02F8	2B	DCX H
02F9	2B	DCX H
02FA	2B	DCX H
02FB	2B	DCX H
02FC	2B	DCX H
02FD	2B	DCX H
02FE	221008	SHLD LDATA
0301	1632	MVI D, 32H
0303	C9	RET

Yes, Load Magnitude

Load End Point

Display Magnitude and Endpoint
Correct LDATA for COMP Routine

Store Maximum Magnitude for COMP
Return

This routine finds the cable end point and displays the average of eight end point values in feet and magnitude.

```

0350 0614      AVG: MVI E,14H
0352 214908    DD1: LXI H,849H
0355 115708    LXI D,857H
0358 0E79      DD2: MVI C,79H
035A 1A        LDAX D
035B 96        SUB M
035C B7        ORA A
035D F26403    JP PLU
0360 2F        CMA
0361 3C        INR A
0362 0E70      MVI C,70H
0364 B8        PLU: CMP B
0365 FAFC03    JM 3FCH
03FC 13        INX D
03FD C37603    JMP NOT
0368 EB        XCHG
0369 221008    SHLD LDATA
036C 322008    STA MAGPT
036F 79        MOV A,C
0370 321208    STA SIGN
0373 C38703    JMP EXT
0376 23        NOT: INX H
0377 7D        MOV A,L
0378 FEDC      CPI 0DCH
037A C25803    JNZ DD2
037D 7C        MOV A,H
037E FE0B      CPI 0BH
0380 C25803    JNZ DD2
0383 05        DCR B
0384 C35203    JMP DD1
0387 1600      EXT: MVI D,00H
0389 3A2008    LDA MAGPT
038C 5F        MOV E,A
038D 2A2108    LHLD ST01
0390 AF        XRA A
0391 19        DAD D
0392 222108    SHLD ST01
0395 11DBF7    LXI D,0F7DBH
0398 2A1008    LHLD LDATA
039B AF        XRA A
039C 19        DAD D
039D 00        NOP
039E 00        NOP
039F 00        NOP
03A0 EB        XCHG
03A1 2A2308    LHLD ST03
03A4 AF        XRA A
03A5 19        DAD D
03A6 222308    SHLD ST03

```

End Point Tolerance

Address of First Data Point

Address of Second Data Point

Load C register with Plus Sign

Load D register Data

Subtract M register Data

Magnitude Positive?

Yes

No, Negative

Load C register with Minus Sign

Compare with End Point Tolerance

Yes

No

Exchange D-E and H-L registers

Store End point Found in H-L

Store Magnitude

Store Sign of Magnitude

End of Data Buffer?

No

No

Yes, Decrement End Point Tolerance

Load Magnitude

Load Magnitude Sum

Add New Magnitude

Store Magnitude Sum

Decode RAM Location to Distance

Load New End Point

Decode to Binary Distance

Load End Point Sum

Add New End Point

Store End Point Sum

03A9	AF	XRA A
03AA	3A1308	LDA M100
03AD	3D	DCR A
03AE	321308	STA M100
03B1	FAB703	JM XX
03B4	C30300	JMP 03H
03B7	2A2308	XX: LHLD ST03
03BA	CD7102	CALL 271H
03BD	221008	SHLD 810H
03C0	2A2108	LHLD ST01
03C3	CD7102	CALL 271H
03C6	0600	MVI B,0H
03C8	4D	MOV C,L
03C9	CD0001	CALL DECODE
03CC	3A1908	LDA ONES
03CF	321508	STA M1
03D2	3A1808	LDA TENS
03D5	321408	STA M10
03D8	3A1708	LDA HUND
03DB	321308	STA M100
03DE	2A1008	LHLD LDATA
03E1	44	MOV B,H
03E2	4D	MOV C,L
03E3	CD0001	CALL DECODE
03E6	CD5501	CALL DISPLA
03E9	C30000	JMP 0000H

Load Counter - Count to 8
Decrement Step Counter

Counter 0?

No

Yes

Call Divide by 8

Store Average Feet

Load Magnitude Sum

Divide by 8

Decode Average Magnitude into
Decimal Digits

Load Distance Average

Decode Average Distance into Decimal
Display Average Feet and Magnitude
Return to Main Program

Chapter 3

OPERATION

The TDRM unit can operate in four major modes: Match, Detect, Average, and Data. For each mode of operation, the TDR waveform is sampled and the data is stored in RAM. Up to 980 points are recorded in RAM and may be extended by the use of additional memory. Each point represents one foot of cable. To insure correct calibration, the cable being tested should be accurately known in length. A non-faulted section of cable should be used to make the calibration setting. Since phase velocities and characteristic impedances vary between the conductors of a multiconductor cable and between different types of cable, failure to make provision for these variations can reduce the absolute accuracy of the TDRM unit. Phase velocities are known to vary between one-half to two-thirds the speed of light for different cables. Cable characteristic impedance is known to vary between 40 to 300 ohms for the typical cables encountered in the mine.

Match Mode - After the unit is turned on the match mode is selected and the reset button is pushed. The Z_0 control is used to match the cable to the TDRM unit. Every two to three seconds a number flashes on the display which is equal to the stored 8 bit data of the sample point approximately 16 feet down the cable. The Z_0 control is used to set this number to 100.

Detect Mode - With the cable matched to the TDRM unit, the detect mode is selected. In a good cable the first major fault would be detected as an open circuit at the end of the cable. Knowing the length of the cable, the Calibrate control is set so that the feet indicated by the first major fault is equal to the length of the cable. The location of subsequent discontinuities shown on the display in decreasing magnitude and increasing

distance are thus located. If this calibration procedure is not performed the discontinuities are proportional to the end point reading given by the first major discontinuity indication. In the detect mode, the magnitude of the discontinuity is displayed in plus or minus quantities to indicate the slope of the discontinuity along with the corresponding feet indication. A positive slope indicates an open circuit, or series resistive fault; a negative slope indicates a short circuit or shunt resistive type fault. The magnitude is only a relative indication of the slope of the discontinuity. Differences among cables and variances in cable connection make it very difficult to relate this number to a meaningful absolute impedance value. Thus the magnitude value is a relative indication of the slope of the discontinuity.

Discontinuities of less than 46 feet cannot be detected in the Detect mode with the first prototype. In the second prototype the Detect 1 mode is used for fault location of distances greater than 50 feet. For discontinuities located at less than 50 feet Detect 2 is used. The first distance in Detect 2 will be shown as 50 feet. Subsequent discontinuities from 1 to 40 feet will be displayed in order of decreasing magnitude and increasing distance.

Average Mode - Because of noise within the TDRM and external noise on the cable, the detect readings on the major discontinuities can vary by plus or minus 4 feet. To reduce this variance of readings, the average mode sums eight of the first readings in the detect mode and displays the average value of the first major discontinuity every 15 to 20 seconds. Averaging reduces readings to plus or minus one foot accuracies.

Data Mode - The Data mode is used to examine the contents of the RAM memory for manual interpretation of the data and TDRM trouble shooting. To allow examination of the data in a section of the cable several 10's or hundreds of feet from the cable beginning, the Fast advance control is depressed until the location of interest is reached at which time data is displayed at a speed slow enough for manual copy.

In the Data mode the number displayed under FEET is the sample point from 1 to 980. The magnitude is a number from 0 to 255 which represents the digitized value of the TDR waveform. Zero represents 0 volts, 255 represents +10V.

Chapter 4

TDRM TESTS

Tests were conducted with the TDRM unit both in the laboratory and on actual coal mine cables in the field. The initial tests have shown that the unit can locate major faults to within plus or minus three feet in the Detect mode and to within plus or minus 1 foot in the Average mode. Further exhaustive tests for at least a year in various environment conditions will be required to verify the performance and usefulness of the TDRM unit.

Multiple conductor cables were found to be the most troublesome, especially when conductors were shorted together in various configurations. Such shorted configuration caused return pulses which reduced the magnitude of discontinuities and subsequently the sensitivity of the TDRM or any other TDR type instrument. Thus care should be taken when connecting the TDRM to the cable under test. Only two cable leads should be connected to the TDRM at any one time and other external leads of the same cable should preferably be left open.

When a cable under test was terminated in its characteristic impedance, either of two possibilities occurred: (1) a minor discontinuity between the actual end of the cable and the point of measurement was detected as a first major discontinuity or (2) the actual end point was detected in a good cable several feet passed the end point. This performance was to be expected. For an ideal cable with no discontinuities and terminated in its characteristic impedance the maximum reading of the TDRM expected for the endpoint would theoretically be an infinity.

The following specific tests represent a sampling of the many tests performed during the development of the TDRM.

4.1 Waveform Tests

Figures 4.1 through 4.4 are TDR waveforms of actual cables as digitized by the TDRM. Fig. 4.1 shows the results to be expected before any power supply isolation was effected for the Sampling Circuitry. As can be seen the noise requires 38 points for stabilization and accuracy is ± 20 feet.

Fig 4.2 shows the end point of a highly capacitive cable at 280 feet. Note the slow rise in TDR waveform after the open circuit. Compare this waveform with that of the 16 gauge 2 conductor cable with an open circuit at 98 feet as shown in Fig. 4.3. The TDR waveform in Fig. 4.3 rises in seven sample points to its final steady state value after the open circuit. The waveform of Fig. 4.2 takes 100 points to reach a steady state value.

Fig. 4.3 also shows the improved sampling performance with isolated power supplies for both computer and sampling circuitry. With the SHM-UH, the TDR waveform takes about 15 points to reach its steady value at the beginning of the TDR pulse. With the SHM-2 about 30 points were required to achieve a steady value at the beginning of the TDR pulse.

Fig. 4.4 shows a short circuit occurring at 37 feet with the 98 foot section of 16 gauge two conductor cable - Note the initial rise time takes place in 3 sample points whereas 13 sample points are required for the digitized value to reach zero.

4.2 Two Conductor Cable Tests

For Fig. 4.3 and 4.4 the adjacent point comparison routine works very well in detecting the end point, major faults and intermediate

discontinuities. Tests using a version of the adjacent comparison routine are shown in Fig. 4.5a and b. Note the variance in end point readings caused by internal circuit noise. The averaging program can reduce this variance from ± 3 feet to ± 1 foot.

In Fig. 4.5a short circuits introduced in the cable can be accurately detected as end points. In Fig. 4.5b a 300Ω shunt fault at 63 feet is detected at 70 feet along with other readings related to the same fault. Such errors in location increase as shunt fault magnitude increases. The 32 ohm series fault at 50 feet is accurately located. Series faults greater than 32 ohms are progressively easier to locate. The lowest series fault resistance that can be detected is approximately 7 ohms.

Fig. 4.6 shows tests performed with the "x point comparison" algorithm where $x = 10$. For 16 gauge 2 conductor cable short circuit location accuracy was found to be the same as in Fig. 4.5. Both the shunt 7 ohm series fault and the 1K shunt fault were also located.

It should be noted that 7 ohm series faults and 1K shunt faults location is only possible under ideal conditions with very low TDRM internal circuit noise and ideal cable matching. Actual in field tests found that a 300 ohm shunt fault was the practical upper limit on detection. A 30Ω series fault was the usual lower limit of detection.

4.3 Multiconductor Trailing Cable Tests

Tests were also conducted at the U.S. Bureau of Mines on a 3 phase, 3 ground round cable which was highly capacitive and repaired in many sections. The cable was measured at 285 feet. Its identification was noted; Hatfield 3 Cond, 4-259 Strand, Type G, 600V, P120 BM, 2-70.

The algorithm used the "x point comparison" technique to locate

both the end point and intermediate discontinuities. X was set equal to 30 to insure positive detection.

The open end point of the cable was found to vary by ± 4 feet when comparing each phase separately to ground. See Fig. 4.7. In comparing the same phase open circuited and short circuited, readings in location were separated by up to 12 feet. This discrepancy in location can be seen by examining Fig. 4.2 which shows the difficulty in accurately locating end points with highly capacitive cables. Also the TDR trace observe on the oscilloscope appeared slightly shorter for the open circuit end point as compared to the short circuit end point.

For a typical set of discontinuity data taken from the TDRM for this cable Fig. 4.7 shows 6 locations with absolute magnitudes greater than 8. The first discontinuity at -9 appears to be located within 10 feet of an equivalent oscilloscope measurement. The remaining four discontinuities of +8 magnitude are arranged in order of increasing distance. Of these the 71 foot point and the 168 foot point was within 10 feet of the measured oscilloscope waveform. The 181 foot point appeared to be due to noise the 249 foot point seem to be a false indication of the end of the cable. The 46 foot point was accurately located within 1 foot of its designation.

As can be seen by this test example a highly capacitive cable with many repairs causes interpretation problems in locating discontinuities. Thus faults greater than 300 ohms would be hidden among the discontinuities already found in the cable. Using a multiconductor flat cable with 3 phase leads and two ground leads, the cable was measured at 205 feet. A short was introduced at 65 feet and was located at 62 feet

as shown in Fig. 4.8. A 50Ω shunt fault at 65 feet was detected at 74 feet as a first discontinuity. A 30Ω shunt fault was detected at 69 feet as a first discontinuity. This indicated that decreasing the value of the shunt fault increased location accuracy.

For a 100Ω shunt fault, location occurred as a second discontinuity point. Location accuracy increased as the shunt fault increased in a value from 100Ω to 400Ω . Above 400 ohms other inherent cable discontinuities concealed the location of the shunt fault.

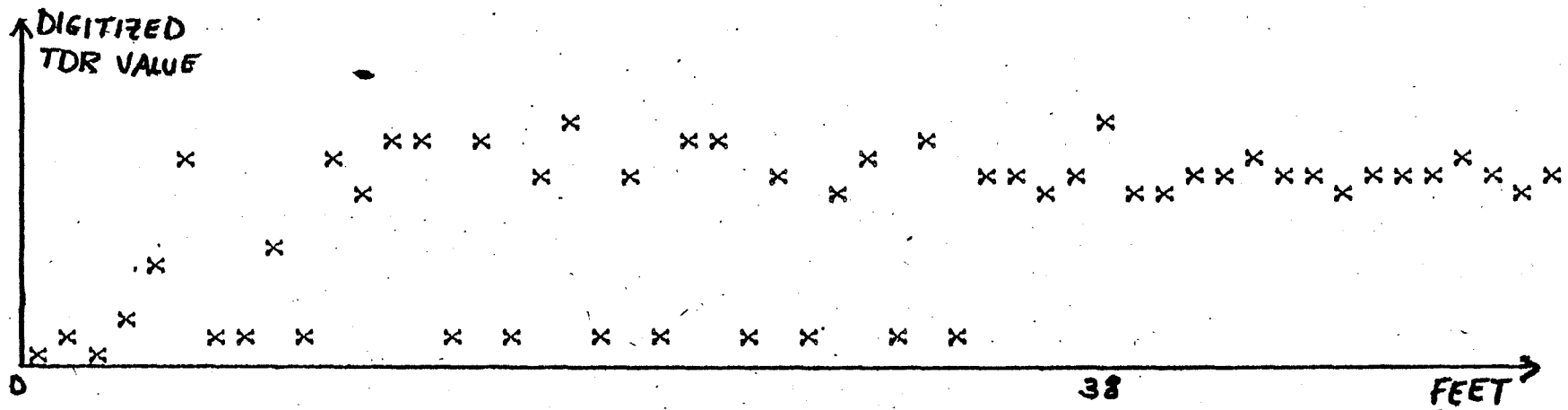


Fig. 4.1 Noisy TDRM Waveform

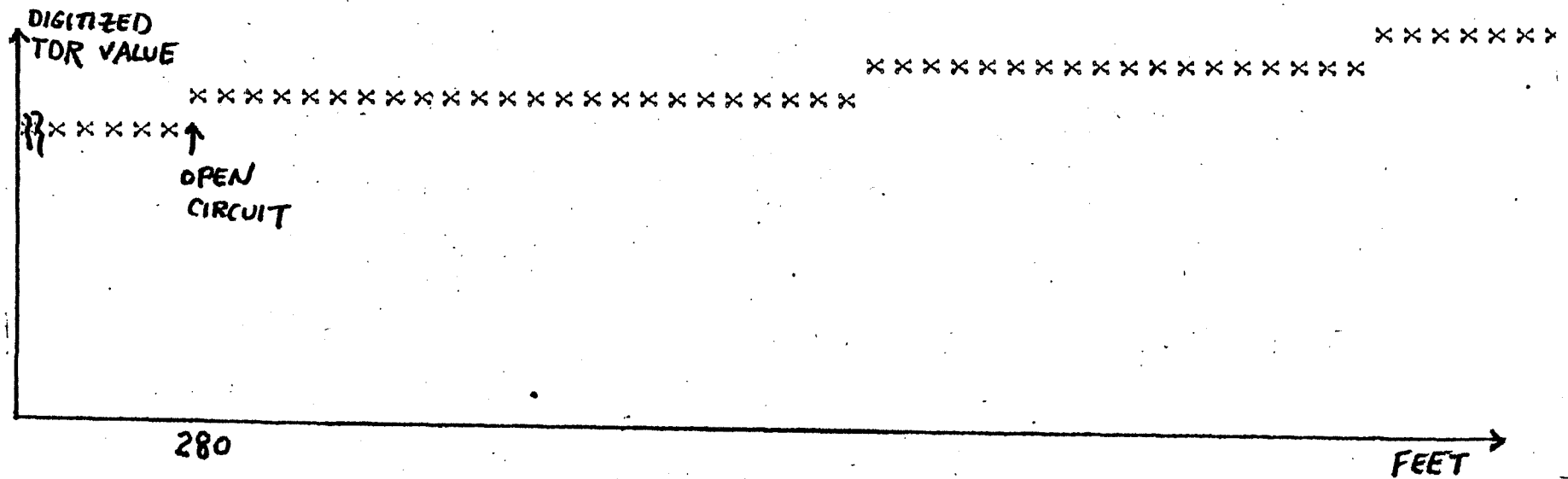


Fig. 4.2 Open Circuit Waveform at End of High Capacitance Cable

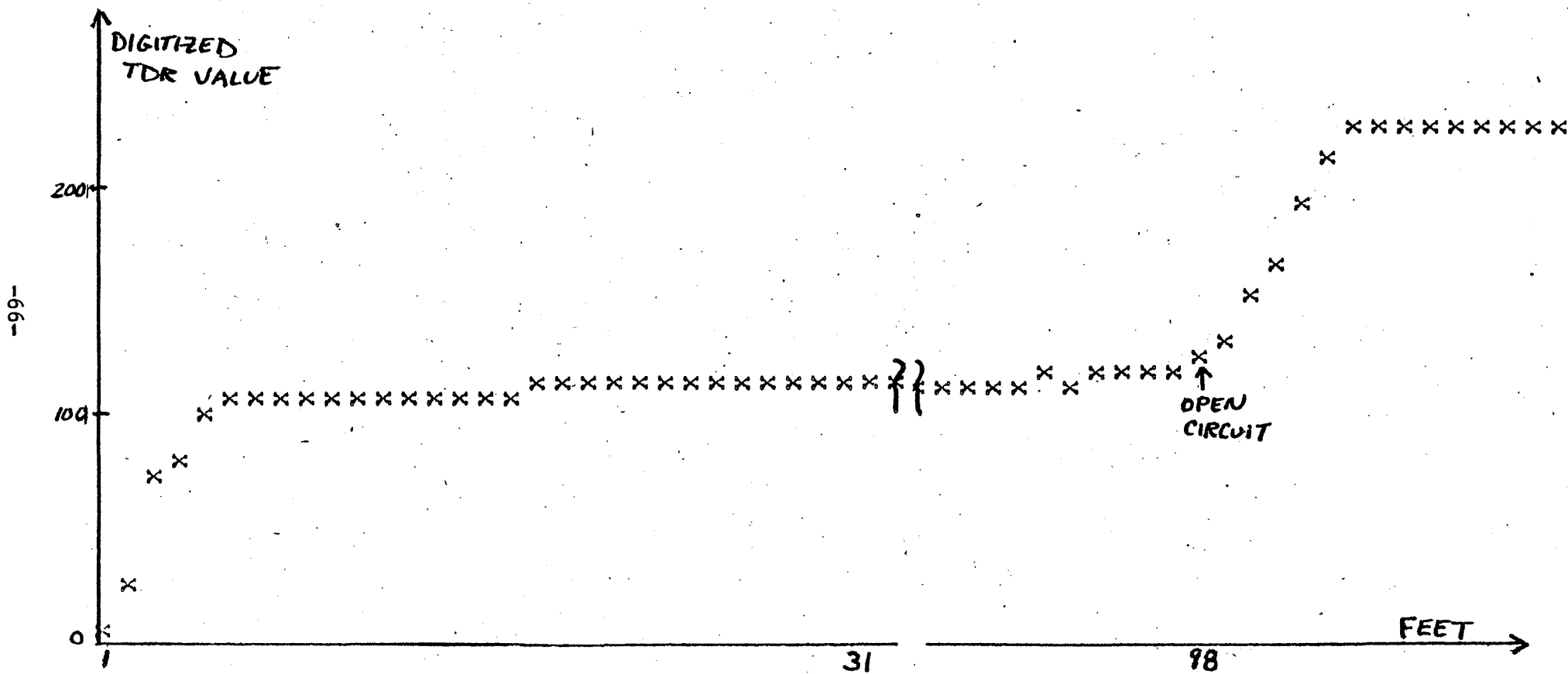


Fig. 4.3 Typical Digital Data to TDRM Open Circuited Cable

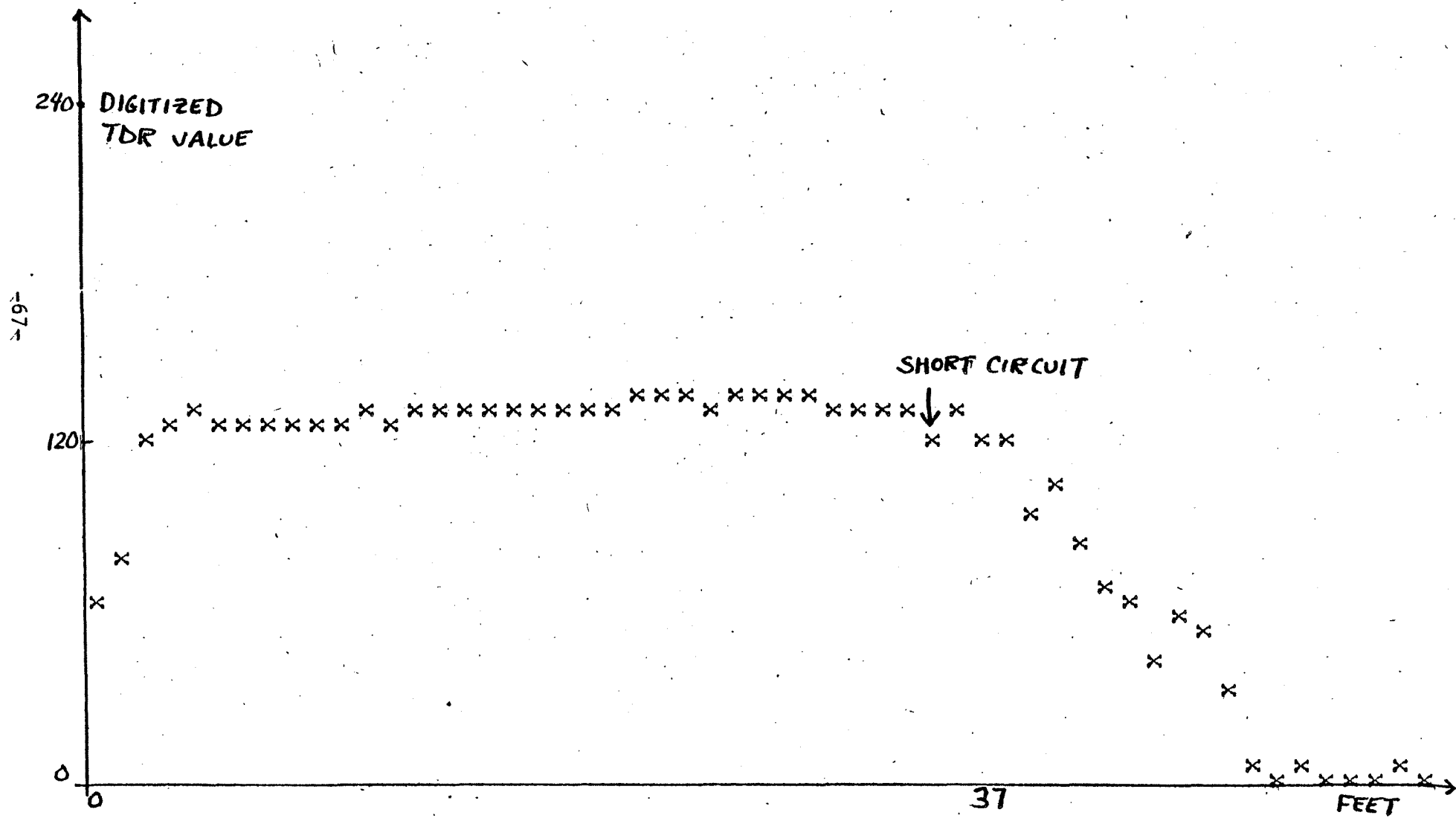


Fig. 4.4 Typical Digital Data to TDRM Short Circuited Cable

TWO CONDUCTOR CABLE TESTS

(Adjacent Point Algorithm)

<u>300 ohm Short at 63 Feet</u>	Magnitude	Feet
	+21	98
	-17	70
	- 9	77
	- 6	72
	- 5	79
	+49	105
	-14	77
	- 8	82
	- 6	75
	- 5	70
	- 5	73
	- 5	77
	+46	100
	-16	71
	-12	78
	- 8	65
	- 7	73
<u>32 ohm Series Fault at 50 Feet</u>		
	+68	102
	+ 8	53
	+ 7	45
	+ 6	47
	+ 6	55
	+29	100
	+15	51
	+ 9	42
	+ 7	54
	+ 7	57
	+47	102
	+15	53
	+ 9	56
	+ 6	47
	+ 5	50

Fig. 4.5(a)

TWO CONDUCTOR CABLE TESTS

(Adjacent Point Algorithm)

Test Cable	50	63	99 Feet
<u>Open at 99 Feet</u>			
	Magnitude	Feet	
	+23	101	
	+47	104	
	+60	100	
	+24	99	
	+22	98	
	+23	100	
	+18	100	
	+29	99	
<u>Short at 99 Feet</u>			
	-43	97	
	-54	98	
	-66	102	
	-48	98	
	-23	98	
	-39	101	
<u>Short at 63 Feet</u>			
	-31	62	
	-31	64	
	-43	64	
	-39	63	
	-38	65	
	-40	64	
<u>Short at 50 Feet</u>			
	-34	51	
	-52	47	
	-27	47	
	-33	50	
	-36	49	
	-36	50	
	-50	50	

Fig. 4.5(b)

TWO CONDUCTOR CABLE TESTS

(X Point Comparison Algorithm, X = 10)

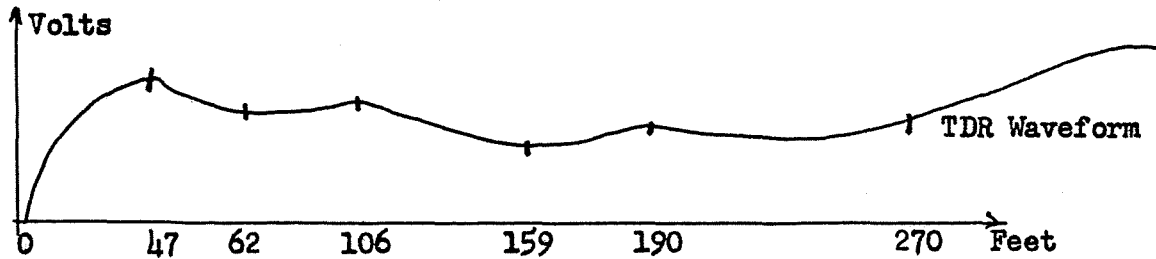
Test Cable	50	62	99 Feet
<u>Short at 62 Feet</u>	Magnitude	Feet	
	-19	61	First Reading in Detect Mode
	-10	64	
	-12	62	
<u>Short at 50 Feet</u>			
	-11	53	First Reading in Detect Mode
	-10	50	
	-13	49	
<u>7 Ohm Series Resistor at 50 Feet, 1 Kilohm Shunt Resistor at 62 Feet</u>			
	+15	99	Readings Made in Detect Mode
	+ 4	45	
	- 4	72	
	+15	101	
	+ 4	52	
	- 4	72	
	+14	100	
	+ 4	48	
	- 4	70	

Fig. 4.6

MULTICONDUCTOR ROUND CABLE TESTS
(Highly Capacitive)

(X Point Comparison Algorithm)

<u>White to Ground (Open)</u>	Magnitude	Feet	Average Mode
	+22	267	
	+22	268	
	+22	267	
<u>Black to Ground (Open)</u>	+22	273	Average Mode
	+22	273	
	+22	272	
<u>Red to Ground (Open)</u>	+21	267	Average Mode
	+21	267	
	+22	266	



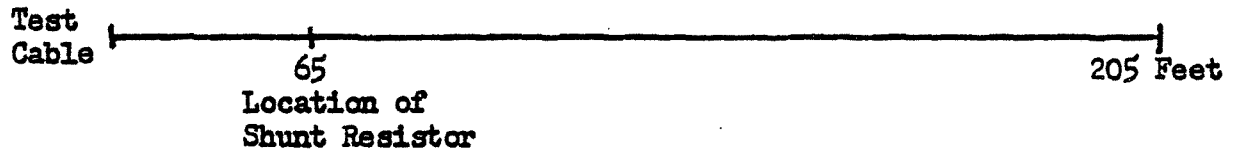
Typical Set of Values
for Intermediate
Discontinuities

Magnitude	Feet	Detect Mode
+24	270	
- 9	116	
+ 8	71	
+ 8	168	
+ 8	181	
+ 8	249	
- 8	46	

Fig. 4.7

MULTICONDUCTOR FLAT CABLE TESTS

(X Point Comparison Algorithm)



<u>Short at 65 Feet</u>	Magnitude	Feet
	-22	62
	-23	62
	-23	62
<u>50 ohm Resistor at 65 Feet</u>		
	-24	74
	-23	74
	-21	73
<u>30 ohm Resistor at 65 Feet</u>		
	-24	69
	-26	71
	-26	71
<u>100 ohm Resistor at 65 Feet</u>		
	+21	206
	-17	85
	-17	87
	-17	88
<u>200 ohm Resistor at 65 Feet</u>		
	+22	200
	- 9	79
	- 9	101
<u>300 ohm Resistor at 65 Feet</u>		
	+23	204
	- 9	73
	- 9	102
<u>400 ohm Resistor at 65 Feet</u>		
	+24	202
	- 9	102
	- 8	74

Fig. 4.8

Chapter 5

CONCLUSIONS

Time Domain Reflectometry can be successfully applied to the detection and location of resistive faults in both shielded and unshielded coal mine trailing cables. The microprocessor-based TDRM unit can successfully locate major faults to within plus or minus one foot, when properly calibrated and used in the Average mode. Such accuracy was found for low capacitance two conductor cable. For high capacitance cable location accuracies of plus or minus five feet were observed.

For low capacitance two conductor cable shunt faults up to 1 Kilohm and series faults greater than 7Ω were detectable with the TDRM. For high capacitance multiconductor cable with splices, shunt faults greater than 300 ohms were usually hidden among the other cable discontinuities caused by the splices.

Noise was one major hardware problem which was remedied by the use of separate power supplies for the sampling circuitry and the microcomputer. Jitter in the TDR sampled waveform causes a variance of plus or minus four feet in the location of the first major discontinuity. Although the Average mode reduces such variation to plus or minus one foot, further hardware improvements would be desirable by the proper location of filter circuits.

Two TDRM prototypes were built. The first prototype used the highly accurate Datel SHM-UH Sample-Hold module with isolated computer and sampling circuit power supplies. The second prototype used the less expensive Datel SHM-2 Sample-Hold module with +5 volt d.c. power supply

isolation being derived from the +15 volt d.c. supply through 7805 voltage regulators. The second prototype accuracy was found to be about twice as poor as the first. The Datel SHM-UH and separate power supplies for computer and sampling circuitry are recommended for any manufactured unit.

Computer misoperation due to overheating of the 8080 microprocessor chip and the PROM's requires the use of either a fan or special chip heat sinks to insure the reliable operation of any manufactured unit. It was found that certain microprocessor chips were more prone to misoperation due to overheating than others. Thus adequate cooling for the computer should be considered before any manufactured unit is finalized in design.

The TDRM prototypes were built with AC to DC power supplied for convenience. Operation is possible from either the conventional 115V_{AC} 60 Hz found at wall outlets or from an inexpensive square wave inverter used with a rechargeable battery.

Several TDRM software programs were written and tested. It was concluded that algorithms comparing the value of a sample point n with that of a sample point $n + x$ were required for highly capacitive cables with slow rates of change in slope at major discontinuities. To achieve higher location accuracy adjacent point (i.e., $x = 1$) comparison techniques were desirable. Of the two prototypes built the first uses the x point comparison technique exclusively with a subsequent inability to detect fault at less than 46 feet. The second prototype uses the x point comparison technique to find the end point and the adjacent point technique to find intermediate discontinuities.

Since the TDRM is software programmed by the use of PROM's, new or optimized program changes can be made to the unit during and after an exhaustive period of field testing with no major hardware changes.

The use of a microcomputer suggests several possible options which can be added to the TDRM unit to enhance or improve operation. The use of a printing unit can be added to give a hard copy of discontinuity results as well as a plot of the sampled TDR waveform data.

If a TDR record were made of each cable before a fault, after a fault and after repair, the fault detection accuracy of the TDRM could be greatly improved. Assuming this comparison technique could be made within the 8 bit accuracy of the present TDRM design, 16 bit A/D conversion could yield fault detection accuracies extending into the megohm shunt resistance range.

To eliminate TDR sampled data jitter, the averaging of many sets of TDR waveforms could be done by lengthening the fast ramp time to allow the computer time to add the new value at each point to a previously accumulated sum for the same point. The final accumulated sum would be divided by the total number of waveforms read to obtain the average point value. Such averaging would be a necessity in any improved fault detection scheme which used magnetic records for before and after comparisons. Also any A/D conversion of greater than 8 bits would require such averaging to justify improved bit accuracy.

REFERENCES

1. "Intel 8080 Microcomputer Systems User's Manual", Intel Corp., Santa Clara, Ca. , July 1975.
2. "The Designers Guide to Programmed Logic", Pro-Log Corp., Monterey, Ca., Dec 1975.
3. "Intel 8080 Assembly Language Programming Manual", Intel Corp., Santa Clara, Ca., 1975.
4. "Intellec 8/MOD 80 Operators Manual", Intel Corp., Santa Clara, Ca., June, 1974.

Appendix A

TIME DOMAIN REFLECTOMETRY (TDR)

The fundamental equations which describe TDR techniques are derived from transmission line theory. Any transmission line can be described by the following two fundamental partial differential equations:

$$-\frac{\partial v}{\partial x} = Ri + L \frac{\partial i}{\partial t} \quad (A-1)$$

$$-\frac{\partial i}{\partial x} = Gv + C \frac{\partial v}{\partial t} \quad (A-2)$$

where v and i are the line voltage and current as defined in Fig. A.1 and

R = resistance per unit length of line

L = inductance per unit length of line

C = capacitance per unit length of line

G = leakage conductance per unit length of line

Using Laplace transformation techniques and solving equations A-1 and A-2 for equations in the form of current only and voltage only the following two equations result:

$$\frac{\partial^2 I}{\partial x^2} - [Ls+R][Cs+G]I = 0 \quad (A-3)$$

$$\text{and } \frac{\partial^2 V}{\partial x^2} - [Ls+R][Cs+G]V = 0, \quad (A-4)$$

where s is the Laplace transform operator

The solutions to equations A-3 and A-4 are:

$$I = A_1 \exp(-nx) + B_1 \exp(nx) \quad (A-5)$$

$$V = A \exp(-nx) + B \exp(nx) \quad (A-6)$$

where A_1 , A_2 , B_1 , B_2 and n are unknowns to be solved for. Equation A-6 is related to equation A-5 through the characteristic impedance $Z_0(s)$. Thus,

$$I = \frac{1}{Z_0} [A \exp(-nx) + B \exp(nx)], \quad (A-7)$$

where

$$Z_0 = \sqrt{\frac{Ls+R}{Cs+G}} = \text{surge impedance} \quad (A-8)$$

For a transmission line of length d terminated in impedance Z_L , with generator impedance Z_G , and an applied pulse whose Laplace transform is $F(s)$, the coefficients of equation A-6 can be solved so that (A-6) becomes:

$$V = \frac{Z_0 F}{Z_G + Z_0} [\exp(-nx) - N \exp(-n(2d-x)) + MN \exp(-n(2d+x)) - MN^2 \exp(-n(4d-x)) + \dots] \quad (A-9)$$

$$\text{where } M = \frac{Z_0 - Z_G}{Z_0 + Z_G} = \begin{array}{l} \text{reflectivity due to generator} \\ \text{impedance mismatch} \end{array} \quad (A-10)$$

$$\text{and } N = \frac{Z_0 - Z_L}{Z_0 + Z_L} = \begin{array}{l} \text{reflectivity due to load} \\ \text{impedance mismatch} \end{array} \quad (A-11)$$

If the generator impedance is matched to the line impedance then $M=0$ and equation (A-9) is simply:

$$V = \frac{F}{2} [\exp(-nx) - N \exp(-n(2d-x))] \quad (A-12)$$

Thus many of the multiple reflections are eliminated by the generator impedance matched to the line impedance Z_0 .

If $F(s)$ is defined, the inverse Laplace transform of (A-12) can be taken to find $v(t)$ at each point x along the transmission line. If only the behavior at $x=0$ is wanted then equation A-12 becomes:

$$V = \frac{F}{2} \left[1 - \frac{Z_0 - Z_L}{Z_0 + Z_L} \exp(-2nd) \right] \quad (A-13)$$

Since Z_0 is a function of s , consider a lossless transmission line where $R=G=0$. Thus

$$Z_0 = \sqrt{\frac{L}{C}} \quad \text{for a lossless line} \quad (\text{A-14})$$

n can be solved for to give: $n = \sqrt{(Ls+R)(Cs+G)} = s\sqrt{LC}$ for a lossless line (A-15)

Also $\sqrt{LC} = \frac{1}{v_p}$ (A-16), where v_p is the phase velocity.

Rewriting equation A-13:

$$V = \frac{F}{2} \left[1 - N \exp\left(-\frac{2sd}{v_p}\right) \right] \quad (\text{A-17})$$

If F is the Laplace transform of a unit step function $v(t)$; i.e., zero voltage for $t < 0$ and unit voltage for $t \geq 0$, then $F(s) = \frac{1}{s}$ and

$$V(s) = \frac{1}{2s} - \frac{N}{2s} \exp\left(-\frac{2sd}{v_p}\right) \quad (\text{A-18})$$

For reflectivity $N=0$; i.e., $Z_L=Z_0$ then the inverse Laplace transformation yields $v(t) = \frac{1}{2} u(t)$ where the output is simply 1/2 the generator input voltage as shown in Figure A.2. If N is some number other than 0 then a reflection takes place which depends upon the transmission line length d and the phase velocity v_p .

For $-1 \leq N \leq +1$

$$v(t) = \frac{u(t)}{2} - \frac{N}{2} u\left(t - \frac{2d}{v_p}\right) \quad (\text{A-19})$$

Thus $v(t)$ is the algebraic summation of a step function beginning at time $t=0$ with that of a step function beginning at a time $t = \frac{2d}{v_p}$ later.

Figures A.2 through A.5 show both the ideal TDR waveform and the actual TDR waveform for the following cases:

- (1) Fig. A.2 shows the response of a coaxial cable to a load Z_L matched to its characteristic impedance Z_0 .
- (2) Fig. A.3 shows the response of the same cable to a short circuited load.

(3) Fig. A.4 shows the response of the same cable to an open circuit.

(4) Fig. A.5 shows the response of a coal mine cable with a 33Ω resistive fault.

It should be noted that the deviations between calculated and observed TDR wave forms are the result of neglecting circuit capacitance and inductance as well as the use of the lossless line approximation. However, the point of discontinuity can always indicate the fault location. Accuracy depends upon the TDR pulse rise-time; thus, the minimum distinguishable distance between two discontinuities is given by the equation:

$$d_{\min} = \frac{v_p t_r}{4} \quad (\text{A-20}), \text{ where}$$

v_p = the phase velocity of the cable $\approx 1.5 \times 10^{10} \frac{\text{cm}}{\text{sec}}$ and t_r = the system rise time.

$$\text{For a 4ns system, } d_{\min} = \frac{1.5 \times 10^{10} \times 4 \times 10^{-9}}{4} = 15\text{cm}.$$

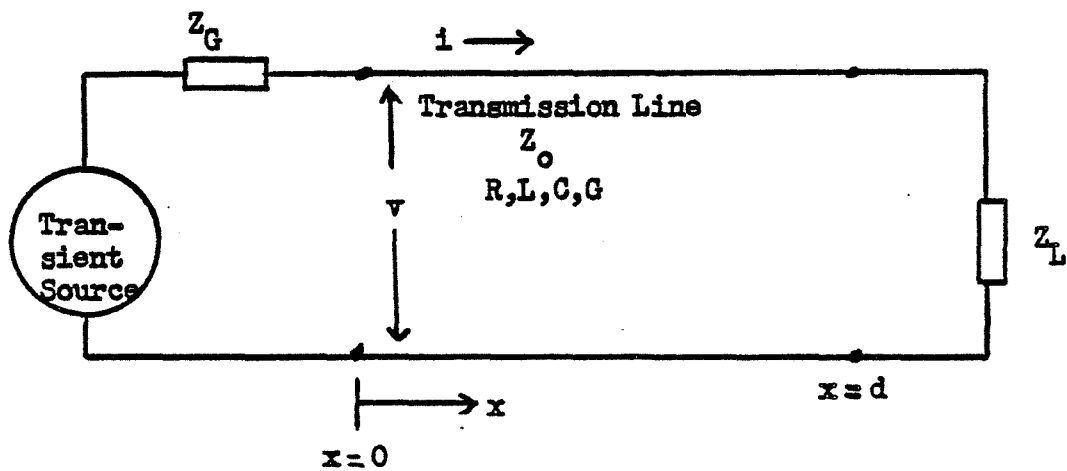
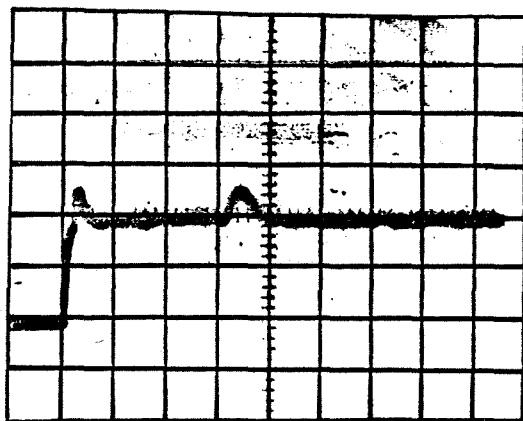


Fig. A.1 Transmission Line Circuit used in Equations of Appendix A.



(Actual)

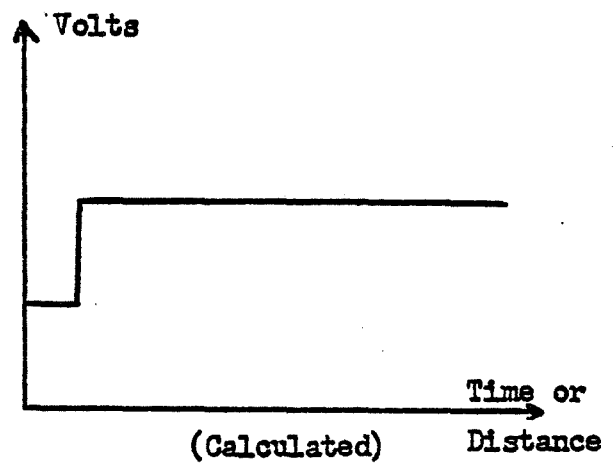
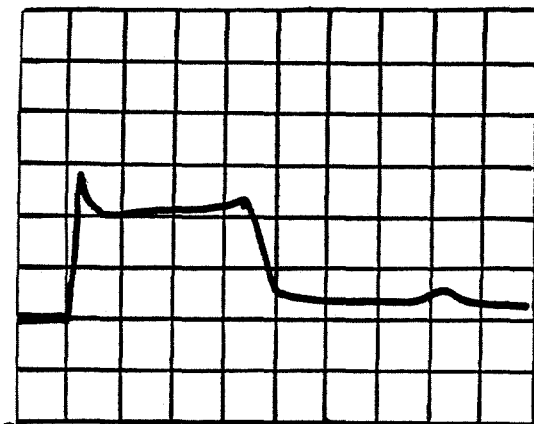


Fig. A.2 TDR Response to a Lossless Coaxial Cable with $Z_L = Z_0$



(Actual)

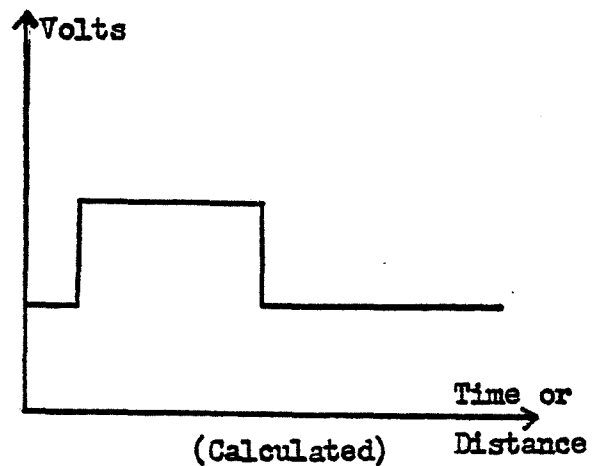
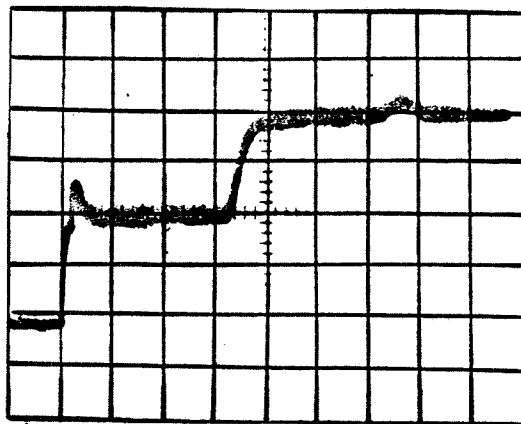
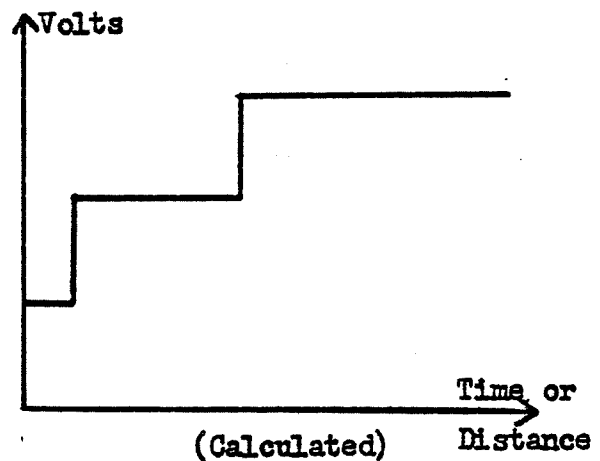


Fig. A.3 TDR Response to a Lossless Coaxial Cable with $Z_L = 0$ ohms.



(Actual)



(Calculated)

Fig. A.4 TDR Response to a Lossless Coaxial Cable with $Z_L = \infty$ ohms.

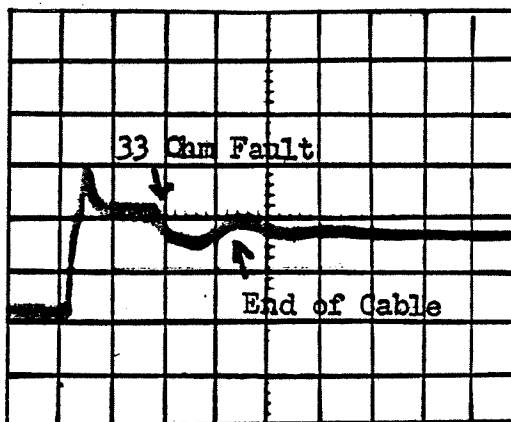


Fig. A.5 TDR Response to a Flat 5 Wire Coal Mine Cable with a 33 ohm Fault 2/3 the distance from the Pulse Transmitter.

Horizontal - 200 nsec./div,
Vertical - 0.5 /div.

APPENDIX B

TDRM OPERATING INSTRUCTIONS

Since the TDRM unit is under continuous software development, the following instructions may be revised at some later date.

The TDRM unit can operate in three major modes: Match, Detect, and Data. For each mode of operation, the TDR waveform is sampled and the data is stored in RAM. Up to 980 points are recorded in RAM and may be extended by the use of additional memory. Each point represents one foot of cable. To insure correct calibration, the cable being tested should be accurately known in length. A non-faulted section of cable should be used to make the calibration setting. Since phase velocities and characteristic impedances vary between the conductors of a multiconductor cable and between different types of cable, failure to make provision for these variations can reduce the absolute accuracy of the TDRM unit. Phase velocities are known to vary between one-half to two-thirds the speed of light for different cables. Cable characteristic impedance is known to vary between 40 to 300 ohms for the typical cables encountered in the mine.

Description of Controls and Switches

ON-OFF Switch - Power Switch

Reset Switch - Initiates software program at PROM address 0000.

Z_0 Control - Matches pulse generator impedance to characteristic cable impedance.

Calibrate Control - Matches sampling circuit timing to cable phase velocity

Mode Switch - Selects desired software program

Fast Display Switch - Enables data to be displayed at faster than normal rate.

TDRM OPERATING INSTRUCTIONS (CONT.)

Description of Operating Modes

Match Mode - After the unit is turned on the match mode is selected and the reset button is pushed. The Z_0 control is used to match the cable to the TDRM unit. Every two to three seconds a number flashes on the display which is equal to the stored 8 bit data of the sample point approximately 16 feet down the cable. The Z_0 control is used to set this number to 100.

Detect Mode - With the cable matched to the TDRM unit, the Detect Mode is selected. In a good cable the only major fault would be detected as an open circuit at the end of the cable. Knowing the length of the cable the Calibrate control is set so that the feet indicated by this major fault is equal to the length of the cable. For example, in Detect 1 mode readings such as 44 feet + 16; 102 Feet -20; 300 Feet +99 might occur. The last reading is the open circuit at 300 Feet. The +99 indicates a 99% open circuit. If the cable were actually 310 Feet, the calibrate control would be adjusted to make this correction.

In the Detect 1 mode all magnitude values less than the absolute value of 16 are not displayed. The Detect 2 mode is used to display all values of magnitude including those less than the absolute value of 16.

The magnitude reading in the Detect mode is approximately proportional to the reflectivity of the cable fault.

Reflectivity is defined as:

$$\rho = \frac{Z_F - Z_0}{Z_F + Z_0}$$

where, ρ is the reflectivity, a number ranging from +1 to -1

Z_0 is the cable characteristic impedance

Z_F is the fault impedance.

TDRM OPERATING INSTRUCTIONS (CONT.)

Thus for $Z_F = 0$ (a short circuit), $\rho = -1.00$. For $Z_F = \infty$ (an open circuit), $\rho = 1.00$. The TDRM unit displays numbers from +.99 to -.99 which can also be interpreted as +99% to -99%.

When calibrated, cable discontinuities are indicated in increasing distance from the pulse source. Because of pulse rise-times, noise and other variables, cables less than 50 Feet should not be used for TDRM Tests.

If a magnitude 99 is encountered in the detect mode, it is assumed that the end of the cable has been reached and no further values are displayed.

If the TDRM output is directly shorted, a 0 Feet - 99 reading will be displayed. If open circuited, the TDRM will display 0 Feet + 99.

Data Mode - The Data mode is used to examine the contents of the RAM memory for manual interpretation of the data and TDRM trouble shooting. To allow examination of the data in a section of the cable several 10's or hundreds of feet from the cable beginning, the Fast advance control is depressed until the location of interest is reached at which time data is displayed at a speed slow enough for manual copy.

In the Data mode the number displayed under FEET is the sample point from 1 to 980. The magnitude is a number from 0 to 255 which represents the digitized value of the TDR waveform. Zero represents 0 volts, 255 represents +10V.

PROCEDURE

1. Determine character of the cable fault by using an ohmmeter to check each combinational pair of cable phase and ground leads. This test will aid in the interpretation and verification of the TDRM data. This test will also indicate whether the fault is an open, short or resistive.

TDRM OPERATING INSTRUCTIONS (CONT.)

2. For cables which do not indicate any fault with an ohmeter, a megger if available and permissible in the testing area should be used to determine if the fault is of a high resistive nature with breakdown occurring at high applied voltages. If this test indicates a high resistive fault then it is unlikely that the present TDRM design will detect this fault.
3. Connect the unfaulted pair of cable leads to the TDRM output.
4. Turn TDRM unit on.
5. Switch to Match Mode with Calibrate control in mid-position.
6. Adjust Z_0 control for a number of approximately 100.
7. Switch to Detect 1 and adjust Calibrate control to match actual cable length. If the cable is open circuited and unfaulted, the cable end would be indicated by a magnitude reading greater than +50.
8. Press Reset and Read all magnitude and feet indications which indicative of cable discontinuities.
9. Switch to Detect 2 for display of all discontinuities.
10. Connect remaining cable pairs and take readings in Detect 1 or Detect 2 modes to locate cable discontinuities.
11. If actual sampled data is to be examined, switch to Data mode. Use the Fast push button to increase display speed if desired.
12. Before effecting repair a tone generator type instrument is recommended for precise fault location.

Examples

The following are typical examples of readings in the Detect 2 mode.

1. 300 Foot Cable with Fault at 120 Feet

a.	<u>Magnitude</u>	<u>Feet</u>	
	+ 1	63	
	+ 3	80	10 ohm fault
	-16	117	
	-86	125	(Fault)

b.	<u>Magnitude</u>	<u>Feet</u>	
	+ 3	81	
	-37	110	(Fault) 100 ohm Fault
	- 1	259	
	+30	294	(End of Cable)

c.	<u>Magnitude</u>	<u>Feet</u>	
	+ 1	64	
	+ 2	85	
	+ 1	99	500 ohm Fault
	- 8	116	(Fault)
	- 1	179	
	+ 1	214	
	+ 7	288	
	+79	305	(End of Cable)

APPENDIX C
TDRM REVISED PROGRAM

In order to improve the previously developed software to indicate fault magnitudes which were more meaningful, the following program was written.

After taking the first difference of all data stored in RAM a new algorithm was developed which was found to be less dependent on cable rise times. Basically the new algorithm:

- (1) Sums all first difference points of like sign.
- (2) If a zero is encountered, up to seven zeros are counted before the program looks for another discontinuity point.
- (3) Starting at the first RAM data location a discontinuity pointer enters the cumulative magnitude of step (1) until a sign change occurs or more than seven zeros are counted.
- (4) At each change in sign of first difference data, the discontinuity pointer advances to that new location.
- (5) All RAM locations between discontinuity points indicate a zero. All discontinuity points indicate the total change in discontinuity magnitude between adjacent discontinuity points.
- (6) Since some slope changes occur in steps, a two point detection routine indicates the first change in slope, while the second point of same slope sign occurs when the first difference point exceeds a threshold value. Such a program variation permits more accurate location of major faults.
- (7) The output magnitude displayed at each discontinuity point ranges from -99% to +99% and is closely related to changes in TDR reflectivity.

TDRM REVISED PROGRAM (CONT.)

- (8) After all discontinuities are analyzed in this manner, a search routine displays the feet and magnitude of all RAM locations of non-zero magnitude. Display is in order of increasing distance. Detect 1 contains a magnitude threshold of 16. Detect 2 contains no magnitude threshold.
- (9) In order to obtain proper performance of the program, both hardware and digital filtering of data are used before first differences are performed.

The attached program printout is the latest revision which uses the new algorithm.

SAMPLE PROGRAM

000	3E8F	MVI A,8FH	Blank Last Digit
002	D301	OUT 1H	
004	311008	LXI SP,810H	Reset Stack
007	212508	LXI H,825H	Memory Start Location
00A	110020	LXI D,2000H	Timing to Determine if Output is Shorted
00D	DE03	IN 3H	Sampling Started?
00F	E602	ANI 02H	No
011	CA0D00	JZ 0DH	Yes, Look for First Meaningful Sample
014	1B	DCX D	
015	DE03	IN 3H	
017	E604	ANI 04H	
019	CA1500	JZ 15H	
01C	DE00	IN 0H	
01E	00	NOP	
01F	FE38	CPI 38H	Start Load Tolerance
021	F23700	JP 37H	Start Load
024	14	INR D	
025	15	DCP D	
026	C21400	JNZ 14H	
029	1C	INR E	
02A	1D	DCR E	
02E	CA3100	JZ 31H	Output Shorted Display 0 -99
02E	C31400	JMP 14H	Try Again
031	3E9D	MVI A,9D	
033	C38700	JMP 87H	
036	00	NOP	
037	DE03	IN 3H	Load Data into RAM
039	00	NOP	
03A	E604	ANI 4H	
03C	CA3700	JZ 37H	
03F	DE00	IN 0H	
041	77	MOV M,A	
042	3EFF	MVI A,FF	RAM Full?
044	BD	CMP L	No
045	C24E00	JNZ 4EH	Maybe
048	3E0E	MVI A,0EH	
04A	EC	CMP H	Yes
04E	CA5200	JZ 52H	No
04E	23	INX H	
04F	C33700	JMP 37H	Matching Mode?
052	DE03	IN 3H	Yes
054	E609	ANI 9H	Data Mode?
056	FE01	CPI 1H	Yes
058	CA0002	JZ 200H	Average Mode
05E	FE08	CPI 8H	Yes, Return to Beginning Mode Non-Existant
05D	CA3202	JZ 232H	No, Go to Next Set of Instructions, Detect Mode
060	FE09	CPI 9H	
062	CA0000	JZ 0H	

DETECT MODE - SEARCH ROUTINE

```

06D 311008 LXI SP,810H
070 0604 MVI B,04H
072 CD9402 CALL 294H
075 05 DCR B
076 3E00 MVI A,0H
078 B8 CMP B
079 C27200 JNZ 72H
07C 213008 LXI H,830H
07F 3E80 MVI A,80H
081 BE CMP M
082 F2BF02 JP 2BFH
085 3E63 MVI A,63H
087 21FE0B LXI H,0BFEH
08A 77 MOV M,A
08B 110000 LXI D,00H
08E C39700 JMP 97H
091 110300 LXI D,03H
094 212A08 LXI H,82AH
097 311008 LXI SP,810H
09A 7E MOV A,M
09B FE00 CPI 00H
09D CA7B03 JZ 37BH
0A0 A7 ANA A
0A1 FAAD00 JM ADH
0A4 4F MOV C,A
0A5 3E79 MVI A,79H
0A7 321208 STA 812H
0AA C3B600 JMP 0B6H
0AD 2F CMA
0AE C601 ADI 01H
0B0 4F MOV C,A
0B1 3E70 MVI A,70H
0B3 321208 STA 812H
0B6 79 MOV A,C
0B7 322108 STA 821H
0BA C36003 JMP 360H

```

Initialize Stack
of Digital Filter Iterations
Average Adjacent Data Points (Filter Data)

Filtering Not Done, Return
Load Memory Pointer

Check if Open Circuit at TDRM Terminals
Cable Connected, Go to Detect Routine

Display 0 +99 Open Circuit

FEET Start
Memory Start
Initialize Stack
Display Faults in Increasing Distance Above Threshold

Fault "+"
Store SIGN

Fault "-"
Store SIGN

```

360 DE02 IN 02H
362 E602 ANI 02H
364 C2C300 JNZ 0C3H
367 79 MOV A,C
368 FE01 CPI 01H
36A C3C600 JMP 0C6H

```

Threshold "1" DETECT 2 Mode

0C3	79	MOV A,C
0C4	FE10	CPI 10H
0C6	FAEF00	JM 0EFH
0C9	FF64	CPI 64H
0CB	FAD000	JM 0D0H
0CE	0E63	MVI C,63H
0D0	0600	MVI B,00H
0D2	CD0001	CALL 100H
0D5	3A1708	LDA 817H
0D8	321308	STA 813H
0DB	3A1808	LDA 818H
0DE	321408	STA 814H
0E1	3A1908	LDA 819H
0E4	321508	STA 815H
0E7	4B	MOV C,E
0E8	42	MOV B,D
0E9	CD0001	CALL 100H
0EC	CD5501	CALL 155H
0EF	23	INX H
0F0	13	INX D
0F1	7D	MOV A,L
0F2	FEFF	CPI 0FFH
0F4	C27003	JNZ 370H
0F7	7C	MOV A,H
0F8	FE0B	CPI 0BH
0FA	C27003	JNZ 370H
0FD	C30000	JMP 00H

Threshold "16" DETECT 1 Mode

DECODE Routine
HUNDREDS
M100
TENS
M10
M1

DECODE Routine
DISPLAY Routine

End of Scan?
No
Maybe
No
Yes

370	3A2108	LDA 821H
373	FE50	CPI 50H
375	FA9A00	JM 9AH
378	C30000	JMP 00H
37B	322108	STA 821H
37E	C3EF00	JMP 0EFH

Threshold for End of Scan Magnitude
No
End of Scan

DECODE ROUTINE

100	E5	PUSH H	
101	D5	PUSH D	
102	69	MOV L,C	
103	60	MOV H,B	
104	97	SUB A	
105	1118FC	LXI D,0FC18H	
108	19	DAD D	
109	24	INR H	
10A	25	DCR H	
10B	FA1201	JM 112H	
10E	3C	INR A	
10F	C30801	JMP 108H	
112	11E803	LXI D,3E8H	
115	19	DAD D	
116	F630	ORI 30H	
118	321608	STA 816H	THOUSANDS
11B	97	SUB A	
11C	119CFF	LXI D,0FF9CH	
11F	19	DAD D	
120	24	INR H	
121	25	DCR H	
122	FA2901	JM 129H	
125	3C	INR A	
126	C31F01	JMP 11FH	
129	116400	LXI D,64H	
12C	19	DAD D	
12D	F620	ORI 20H	
12F	321708	STA 817H	HUNDREDS
132	97	SUB A	
133	11F6FF	LXI D,0FFF6H	
136	19	DAD D	
137	24	INR H	
138	25	DCR H	
139	FA4001	JM 140H	
13C	3C	INR A	
13D	C33601	JM 136H	
140	110A00	LXI D,0AH	
143	19	DAD D	
144	F610	ORI 10H	
146	321808	STA 818H	TENS
149	7D	MOV A,L	
14A	F600	ORI 00H	
14C	321908	STA 819H	ONES
14F	D1	POP D	
150	E1	POP H	
151	C9	RET	

DISPLAY ROUTINE

155	E5	PUSH H	
156	3A1308	LDA 813H	
159	E60F	ANI 0FH	M100 Equals 0?
15B	CA6901	JZ 169H	Yes, Blank It
15E	F660	ORI 60H	No, Fix Code
160	321308	STA 813H	
163	3A1408	LDA 814H	
166	C37601	JMP 176H	
169	3E8F	MVI A, 8FH	Blank M100
16E	321308	STA 813H	
16E	3A1408	LDA 814H	
171	E60F	ANI 0FH	M10 Equals 0?
173	CA7B01	JZ 17BH	Yes, Blank It
176	F650	ORI 50H	No, Fix Code
178	C37D01	JMP 17DH	
17B	3E8F	MVI 8FH	Blank M10
17D	321408	STA 814H	
180	3A1508	LDA 815H	
183	E60F	ANI 0FH	
185	F640	ORI 40H	Fix Code for M1
187	321508	STA 815H	
18A	3A1608	LDA 816H	
18D	E60F	ANI 0FH	Blank THOU?
18F	C2B101	JNZ 1B1H	No
192	3E8F	MVI 8FH	
194	321608	STA 816H	
197	3A1708	LDA 817H	
19A	E60F	ANI 0FH	Blank HUND?
19C	C2B101	JNZ 1B1H	No
19F	3E8F	MVI 8FH	
1A1	321708	STA 817H	
1A4	3A1808	LDA 818H	
1A7	E60F	ANI 0FH	Blank TENS
1A9	C2B101	JNZ 1B1H	No
1AC	3E8F	MVI A, 8FH	
1AE	321808	STA 818H	
1B1	210020	LXI H, 2000H	Load Display Time Counter
1B4	DB02	IN 02H	
1B6	E601	ANI 01H	Fast Display?
1B8	C2BE01	JNZ 1BEH	No
1BB	210001	LXI H, 100H	Yes, Reload Display Time Counter for Fast Display

1BE	3A1208	LDA 812H	OUTPUT SIGN
1C1	D301	OUT 1H	
1C3	3A1308	LDA 813H	OUTPUT M100
1C6	D301	OUT 1H	
1C8	3A1408	LDA 814H	OUTPUT M10
1CB	D301	OUT 1H	
1CD	3A1508	LDA 815H	OUTPUT M1
1D0	D301	OUT 1H	
1D2	3A1608	LDA 816H	OUTPUT THOU
1D5	D301	OUT 1H	
1D7	3A1708	LDA 817H	OUTPUT HUND
1DA	D301	OUT 1H	
1DC	3A1808	LDA 818H	OUTPUT TENS
1DF	D301	OUT 1H	
1E1	3A1908	LDA 819H	OUTPUT ONES
1E4	D301	OUT 1H	
1E6	3E8F	MVI A, 8FH	BLANK
1E8	D301	OUT 1H	
1E9	00	NOP	
1FA	00	NOP	
1EB	00	NOP	
1EC	00	NOP	
1ED	00	NOP	
1EE	00	NOP	
1EF	00	NOP	
1F0	00	NOP	
1F1	97	SUB A	
1F2	2B	DCX H	
1F3	B5	ORA L	
1F4	C2BE01	JNZ 1BEH	
1F7	B4	ORA H	
1F8	C2BE01	JNZ 1BEH	
1FB	E1	PDP H	
1FC	C9	RET	

MATCH ROUTINE

```

200 0600 MVI B,00
202 3A3508 LDA 835H
205 4F MOV C,A
206 CD0001 CALL 100H
209 3A1908 LDA 819H
20C 321508 STA 815H
20F 3A1808 LDA 818H
212 321408 STA 814H
215 3A1708 LDA 817H
218 321308 STA 813H
21B 3E8F MVI A,8FH
21D 321208 STA 812H
220 321608 STA 816H
223 321708 STA 817H
226 321808 STA 818H
229 321908 STA 819H
22C CD5501 CALL 155H
22F C30000 JMP 00H

```

Match Location

DECODE Routine

ONES

ML

TENS

MLO

HUND

MLOO

BLANK

DISPLAY ROUTINE

DISPLAY ROUTINE

```

232 3E3F MVI A,8FH
234 321208 STA 812H
237 110100 LXI D,01H
23A 212508 LXI H,825H
23D 0600 MVI B,00H
23F 4E MOV C,M
240 CD0001 CALL 100H
243 3A1908 LDA 819H
246 321508 STA 815H
249 3A1808 LDA 818H
24C 321408 STA 814H
24F 3A1708 LDA 817H
252 321308 STA 813H
255 42 MOV E,D
256 4E MOV C,E
257 CD0001 CALL 100H
25A CD5501 CALL 155H
25D 13 INX D
25E 23 INX H
25F 3E00 MVI A,00H
261 ED CMP L
262 C23D02 JNZ 23DH
265 3E0C MVI A,0CH
267 EC CMP H
268 C23D02 JNZ 23DH
26E C30000 JMP 00H
26E 00 NOP

```

Blank SIGN

Initialize FEET COUNTER

Initialize MEMORY START Address

MOVE Memory to Decode

Call DECODE Routine

ONES

ML

TENS

MLO

HUND

MLOO

DECODE Routine

DISPLAY Routine

Increment FEET

End of Data?

No

Maybe

No

Yes, Go to SAMPLE

DIVIDE BY TWO ROUTINE

271	AF	XPA A
272	78	MOV A, B
273	0F	RFC
274	00	NOP
275	47	MOV B, A
276	AF	XPA A
277	79	MOV A, C
278	0F	RFC
279	00	NOP
27A	E67F	ANI 7FH
27C	4F	MOV C, A
27D	78	MOV A, B
27E	E680	ANI 80H
280	B1	OFA C
281	4F	MOV C, A
282	78	MOV A, B
283	E67FH	ANI 7FH
285	47	MOV B, A
286	C9	RET

ADD TWO NUMBERS TOGETHER ROUTINE

287	1600	MVI D, 00H
289	5E	MOV E, M
28A	EB	XCHG
28B	D5	PUSH D
28C	AF	XPA A
28D	09	DAD B
28E	D1	POP D
28F	EB	XCHG
290	4B	MOV C, E
291	42	MOV E, D
292	23	INX H
293	C9	RET

FILTER DATA ROUTINE

294	C5	PUSH B
295	212503	LXI H, 825H
298	010000	LXI B, 00H
29B	CD8702	CALL 287H
29E	CD8702	CALL 287H
2A1	2B	DCX H
2A2	2B	DCX H
2A3	CD7102	CALL 271H
2A6	71	MOV M, C
2A7	23	INX H
2A8	7D	MOV A, L
2A9	FEFF	CPI 0FFH
2AB	C29802	JNZ 298H
2AE	7C	MOV A, H
2AF	FE0E	CPI 0EH
2B1	C29802	JNZ 298H
2B4	01	POP B
2B5	C9	RET
2B6	00	NOP

SLOPE CHANGE ROUTINE

2BF	97	SUB A	Zero A Register
2C0	322208	STA 822H	Store in Zero Counter
2C3	212508	LXI H, 825H	Initialize Memory
2C6	23	INX H	
2C7	7E	MOV A, M	Load D_{x+1} into Memory
2C8	2B	DCX H	
2C9	96	SUB M	Take First Difference $D_{x+1} - D_x$
2CA	77	MOV M, A	Store in Location x
2CB	23	INX H	Increment x by 1
2CC	7D	MOV A, L	End of Memory?
2CD	FEFF	CPI 0FFH	No
2CF	C2C602	JNZ 2C6H	Maybe
2D2	7C	MOV A, H	
2D3	FE0B	CPI 0BH	No
2D5	C2C602	JNZ 2C6H	Yes, Initialize First Difference Pointer
2D8	212608	LXI H, 826H	Initialize Discontinuity Pointer
2DB	112508	LXI D, 825H	Initialize 2 Point Counter
2DE	0E00	MVI C, 00	Move First Difference to A Register
2E0	7E	MOV A, M	First Difference Equals 0?
2E1	FE00	CPI 00H	Yes, Jump to ZERO Routine
2E3	CA8103	JZ 381H	No, First Difference Plus or Minus?
2E6	A7	ANA A	Minus
2E7	FA1503	JM 315H	Plus
2EA	47	MOV B, A	Load A register with Cumulative First Diff. Data
2EB	1A	LDAX D	Cumm. First Diff. Data Plus or Minus?
2EC	A7	ANA A	Minus
2ED	FA3003	JM 330H	Plus
2F0	3E01	MVI A, 01H	Looking for 2nd Discontinuity Point?
2F2	B9	CMP C	Yes
2F3	CA4103	JZ 341H	No
2F6	3E02	MVI A, 02H	Compare if First Difference Greater than Threshold
2F8	B8	CMP B	Yes
2F9	FA4E03	JM 34BH	No
2FC	C34103	JMP 341H	Load A Register with Cum. First Diff. Data
2FF	1A	LDAX D	Add First Diff. Data of Same Sign
300	86	ADD M	Store Data at Discontinuity Pointer
301	12	STAX D	Zero First Diff. Pointer Location
302	3E00	MVI A, 00H	
304	77	MOV M, A	Increment First Diff. Pointer
305	23	INX H	Compare if end of RAM
306	7D	MOV A, L	
307	FEFF	CPI 0FFH	No, Continue
309	C2E002	JNZ 2E0H	Maybe
30C	7C	MOV A, H	
30D	FE0B	CPI 0BH	No, Continue
30F	C2E002	JNZ 2E0H	Yes, Jump to SEARCH ROUTINE
312	C39100	JMP 91H	

315	2F	CMA
316	C601	ADI 01H
318	47	MOV B,A
319	1A	LDAX D
31A	A7	ANA A
31B	FA2103	JM 321H
31E	C33003	JMP 330
321	3E01	MVI A,01
323	E9	CMP C
324	CAFF02	JZ 2FFH
327	3E02	MVI A,02H
329	E8	CMP B
32A	FA3703	JM 337H
32D	C3FF02	JMP 2FFH
330	0E00	MVI C,00H
332	5D	MOV E,L
333	54	MOV D,H
334	C30503	JMP 305H
337	0E01	MVI C,01H
339	1A	LDAX D
33A	5D	MOV E,L
33B	54	MOV D,H
33C	86	ADD M
33D	77	MOV M,A
33E	C30503	JMP 350H
341	1A	LDAX D
342	86	ADD M
343	FE7A	CPI 7AH
345	FA0103	JM 301H
348	C33003	JMP 330H
34B	0E01	MVI C,01H
34D	1A	LDAX D
34E	5D	MOV E,L
34F	54	MOV D,H
350	86	ADD M
351	FE7A	CPI 7AH
353	FA3D03	JM 33DH
356	3E7A	MVI A,7AH
358	C33D03	JM 33DH

Absolute Value

Load A Register with Cum. First Diff. Data
Cum. First Diff. Data Plus or Minus?
Minus
Plus

Looking for 2nd Discontinuity?

Yes

No

Compare if First Discontinuity > than Threshold

Yes

No

Reset Second Discontinuity Counter

Transfer New Discontinuity Location from HL TO
DE Registers

Set Discontinuity Counter to 1

Load A Register with CUMM First Diff. Data

Transfer New Discontinuity Location from HL to
DE Registers

Add First Diff Data to A Register

Load A Register with Cumm First Diff. Data

Add First Diff Data of Same Sign

Cum First Diff Data > than Max. Positive Number?

No

Yes

Load C register to show 2nd Point found

Load A register with Cum First Diff Data

Transfer New Discontinuity Location from HL to
DE Registers

Add First Diff Data to A Register

Compare if 2nd Discontinuity Positive No. MAX

No

Yes

ZERO ROUTINE

381	23	INX H	Increment First Diff. Pointer
382	7E	MOV A,M	
383	2B	DCX H	Decrement Pointer
384	FE00	CPI 00H	Compare if Zero?
386	C29C03	JNZ 39CH	Not Zero
389	3A2208	LDA 822H	Yes
38C	3C	INR A	Increment Zero Counter
38D	322208	STA 822H	
390	FE07	CPI 7H	Compare if Zero Counter Equal Max Count
392	C25003	JNZ 350H	No
395	97	SUB A	Yes
396	322208	STA 822H	Set Zero counter to 0
399	C33003	JMP 330H	
39C	97	SUB A	
39D	322208	STA 822H	
3A0	C35003	JMP 350H	

APPENDIX D

FMC - TDR Unit Modifications

INTRODUCTION

This report summarizes the work done on Phase 1 of U. S. Bureau of Mines Contract No. H0346138, "Cable Fault Location at Elevated Voltage Level." The contents of this report will be included in the Final Report in an expanded format.

Phase 1 of Contract No. H0346138 was devoted to modification of the FMC Model 302A Cable Fault Locator to:

1. Increase pulse voltage from a maximum of 4 volts to 40 volts in the TDR mode
2. Increase sensitivity of the Cable Fault Locator to detect to a wider range of resistive faults in the TDR mode
3. Possibly improve accuracy of fault location to a value better than the original ± 15 feet
4. Increase the output voltage level of the oscillator when operated in the electromagnetic/electrostatic mode

Preliminary tests conducted during a feasibility study indicated that pulse voltage levels between 10 to 40 volts peak were adequate in detecting nonlinear faults. Voltages between 40 and 300 volts peak did not reduce nonlinear fault resistances appreciably to justify the added circuitry costs. Although impulse voltages between 5 kV to 15 kV would be the ultimate improvement to a fault locator, they are not suitable for underground mine use and such instruments are already commercially available. Thus, the modified cable fault locator is designed for use in underground mines for the location of trailing cable faults.

The TDR mode provides an initial indication of fault location and type on trailing cables of up to 1,000 feet in length. Accuracy in this mode is ± 10 feet. Final location is accomplished by the use of a 10-kHz oscillator with an external electrostatic/electromagnetic probe capable of precisely pin pointing the faulted section of cable.

DESCRIPTION OF MODIFICATIONS

The changes to the FMC Model 302A Cable Fault Locator are shown in the Block Diagram of Figure 1. In Figure 1A, modifications in the TDR mode were made to the clock circuitry and detection sensitivity circuits. In addition, a pulse amplifier was added to produce 40-volt peak pulses and an attenuator was added to make the reflected pulses compatible with the 5-volt TTL detection circuitry.

In the electrostatic/electromagnetic mode, a simple transformer coupled amplifier was added to the MC4024 oscillator to increase open circuit output voltage.

Figure 2 is a detailed schematic of the modifications as exist in the CMU prototype. Modifications to the clock circuitry include a change in C_7 to 10 pF and the addition of a 500- Ω trim resistor RA. The 10-pF capacitor increases the clock frequency to improve sensitivity of fault location to ± 10 feet. Further increases are not possible with the TTL components as used. The trim potentiometer RA was added to provide an adjustment to the clock frequency via the voltage controlled oscillator terminal of UI. Such a trim was found to improve the performance of units and make adjustments for unit to unit deviations. If

RA were not used in a final manufactured product, terminal 12 should be tied to the +5-volt bus rather than being left to float as originally designed.

The pulse amplifier includes the addition of a 45-volt XX30 "B" battery with changes to components Q6 and R16 and the addition of transistor QA. Transistor Q6 is a high-speed, high-current PNP device which derives its emitter power from the 45-volt battery directly. Additional drive for Q6 is provided by QA which operates in a Darlington configuration with Q6. Because of the increased operating voltage levels, R16 was increased to 220 Ω to reduce the voltage reference levels applied to U5, the 9615 line receiver.

The attenuation circuitry includes changes to resistor R16 as previously noted and the addition of resistors RB and RC. Resistor RB is 1 k, 1/2 watt and operates as a voltage divider in series with RC, a 500- Ω 1/2-watt trimpot. The trimpot is set to approximately 100 Ω and could possibly be replaced in any final manufactured product by its set value.

Resistor R17 controls the sensitivity of the cable fault locator to resistance faults. Reduction to 0 ohms is possible for the highest sensitivity; however, a final manufactured model would probably use a value of 1/2 ohm or so to provide circuit stability.

Resistor R19 was changed to 33 Ω to prevent excessive dissipation by transistor Q6 should the TDR output terminals be directly shorted.

The modification to the 10-kHz oscillator circuit uses only the 10-kHz signal produced by U1 at terminal 6. A small vector board was

mounted within the prototype unit which contains transistors QB, QC and QD and resistors RD and RE. All transistors are type 2N3053.

The 10-kHz signal from UI is voltage amplified by QB and RD and is current amplified by the emitter follower circuit of QC-QD (a Darlington arrangement) in series with RE and the 25.2-V winding of transformer T1. Both QC and QD must be heat sunked using the standard T05 fin types. Added power can be obtained by the substitution of a 2N6386 power Darlington for transistor QC and QD with the removal of RE. The power Darlington must be heat sunked to the chassis in this case.

Although a 25-VA transformer was used, a smaller type could be designed by taking advantage of the 10-kHz operating frequency. The present type was chosen because it is a standard off-the-shelf item.

The 10-kHz oscillator amplifier circuitry was kept separate from the TDR circuitry in the prototype unit to eliminate interference between the two circuits. Proper arrangement in a manufactured unit could share the same output terminals. Also, a line selector switch with five clip leads could be used in the final manufactured version similar to the original FMC Model 302A.

Since transistor Q2 dissipates considerable power during operation, it should be heat sunked using the slip on T05 fin type heat sinks as used in the prototype.

A list of components necessary for the manufacture of the modified cable fault locator are listed in Figure 3.

GENERAL SPECIFICATIONS OF MODIFIED PROTOTYPE

TDR Mode:

Pulse voltage	+40 volts
Pulse duration	2 μ sec. min., 4 μ sec. max.
Pulse frequency	5 pulses/sec.
Pulse rise time	20 nanosec.
Pulse power	.25 milliwatts max. into 33- Ω load
Location sensitivity	$\pm$ 10 feet
Resistance sensitivity	0 to 60 Ω , 130 to ∞ for faults located at end of 100- Ω cable*
Cable characteristic impedance adjustment	33 to 133 Ω
Short circuit light	operates for faults less than cable characteristic impedance
Open circuit light	operates for faults greater than cable characteristic impedance

Electrostatic/Electromagnetic Mode:

Pulse voltage	40 volts peak-to-peak open circuit 6 volts peak-to-peak into 100- Ω load
Pulse frequency	10 kHz
Pulse power	40 milliwatts into 100- Ω load
Operates with FMC Model 352A pick-up	

General:

Power supplies	6-volt, CD-33 Ni-Cad recharge- able battery 45-volt, XX30 "B" battery
Component availability	Both Motorola and Texas Instruments can be used interchangeably as

*Note faults located within a 100- Ω cable can also be detected in 60- to 200- Ω range with proper interpretation of instrument readings.

required. Texas Instruments also
second sources Fairchild's 9615.

OPERATION AND ADJUSTMENTS

Internal Adjustments (Done Only When Manufactured):

1. RC should be set for approximately 100 Ω .
2. RA should be approximately zero Ω between pins 12 and 13 of UI.
3. Turn unit on to TDR with clip leads plugged into TDR output terminals.
4. Set Z_0 control approximately 2/3 counterclockwise.
5. Adjust RA for highest number.
6. Short out clip leads -- short light should go on.
7. Open clip leads -- open light should go on.
8. If not, RC should be adjusted slightly.

External Adjustments and Operation:

1. Connect the clip leads to the TDR terminals and a length of good cable of same type as to be tested.
2. Turn unit switch to TDR.
3. Adjust Z ADJ for maximum number reading (approximately 6 for a 100-foot cable of 100- Ω characteristic impedance.
4. Short end of cable and observe that short light is illuminated and display number either stays the same or changes at most by one number, readjust Z ADJ if necessary.

5. Open circuit cable and observe open light is illuminated.
6. Remove cable and observe number indication with clip leads alone (usually a 1 or 2). This number will be subtracted from any future readings.
7. Thus, if number for a 100-foot cable open or short is 7 and for the clip leads is 2, then each 100-feet of cable contributes 5 to the display or each 20 feet contributes a 1.
8. Using the scaling factor as in step 7, the faulted cable can now be tested. If the TDR would show a 5 short for the same cable as in step 7, then a short would exist at $(5 - 2) \times 20 \text{ feet} = 60 \text{ feet}$ from the TDR clip leads.
9. Usually 3 or more leads are observed in coal mine trailing cable. In this case, only one is usually bad or shorted to ground. Thus, the highest number is set using Z ADJ on a good pair. Correction for this number is made by subtracting the clip lead reading. Now the faulted cable section is connected. Z ADJ is again adjusted for the highest reading. A short indicates a fault of less than characteristic impedance. An open may be a fault indication only if the new number is less than the previous number. The fault is now located by comparison, i.e.,

$$(\text{FAULTED \#} - \text{CLIP LEAD \#}) / (\text{UNFAULTED \#} - \text{CLIP LEAD \#})$$

$$\times \text{TOTAL LENGTH OF CABLE.}$$

Example:

FAULTED # = 8

UNFAULTED # = 51

CLIP LEAD # = 1

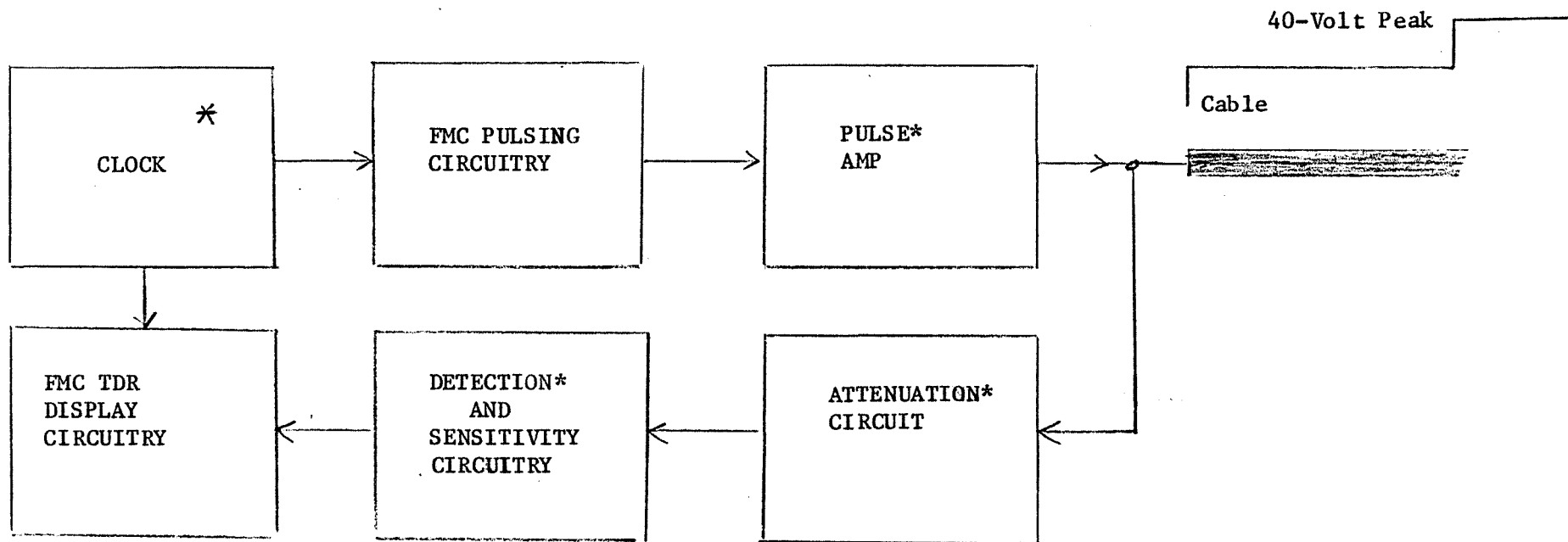
Therefore:

$$\frac{8 - 1}{51 - 1} \times \text{length} = \frac{7}{50} \text{ of length of cable}$$

Faults are now precisely located using electrostatic/electromagnetic techniques:

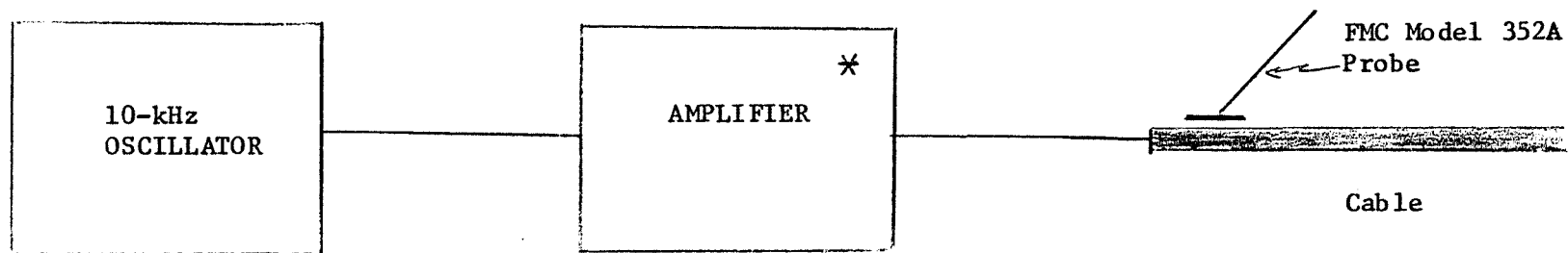
1. Connect clip leads to OSC terminals.
2. Turn switch on to OSC.
3. Yellow light should be on.
4. Connect clip leads to faulted cable.
5. Use FMC Model 352A pickup on open setting for open and short setting for shorts.
6. Scan cable with pickup at approximate location given by TDR.
 - a. An open will be indicated by a sudden loss of signal.
 - b. A short will be indicated by a sudden change or dip in meter reading.
7. The fault should now be repaired.

NOTE: Faults within 60- to 200- Ω range may be located by TDR techniques by use of the Z_o adjust control. As the control is varied, three separate readings should be observed. The highest represents the end of the cable. The lowest is caused by improper cable matching and the intermediate steady reading would be the fault location.



*Modifications

A. TDR MODE



B. ELECTROSTATIC/ELECTROMAGNETIC MODE

FIGURE 1: CABLE FAULT LOCATOR MODIFICATION BLOCK DIAGRAM

Figure 2 is a CMU modification to FMC Drawing No. 5110313. Because of its size it is not included here, but may be obtained from the U.S. Bureau of Mines, Pittsburgh, Pa.

Additional Parts Needed for Modification of FMC TDR to Elevated Voltage Unit with Increased Sensitivity to Resistive Faults: (Ref. U. S. B. M. Contract Number 0346138, FMC Drawing 5110310)

- 1 - 2N3720 Transistor
- 3 - 2N3053 Transistors
- 1 - 390- Ω , 1/2-watt Resistor, 5%
- 1 - 10- Ω , 2-watt Resistor, 5%
- 3 - T05 Heat Sinks, Type 2230B-5, Allied Radio 957-2190
- 1 - 220- Ω , 1/2-watt Resistor, 5%
- 1 - 1-k, 1/2-watt Resistor, 5%
- 1 - 47- Ω , 1/2-watt Resistor, 5%
- 1 - 1-k, 1/2-watt Trimpot, Micropot 3805k-1k (Allied 714-82035)
- 1 - 100- Ω , 1/2-watt Trimpot, Micropot 3805k-100 (Allied 714-8220)
- 1 - Battery 45 volt, Burgess XX30
- 1 - Transformer, Allied Type 6K37HF, 25.2 volts at 1.0 amp., 120 volts Prim. or Equiv. ~ \$5.63
- 1 - New P.C. Board Layout, Approximately 5x5 with Double Sided Copper, 10 Glass Epoxy
- 1 - New Chassis to Hold Items BUD 736-2501 or Equiv.

FIGURE 3

Carnegie-Mellon University

Department of Electrical Engineering
Schenley Park
Pittsburgh, Pennsylvania 15213
[412] 621-2600

Ref: U.S. Bureau of Mines Contract No. H0346138

SUBJECT: February 1976 Monthly Progress Report

Phase 1 MODIFIED FMC FAULT LOCATOR

Four prototype units were delivered to the U.S. Bureau of Mines by Preisser-Mineco. Only one of the four units functioned in the TDR mode. Three of the malfunctioning units were given to CMU for test and analysis.

It was found that a 500 ohm trimpot added to replace the fixed 220 Ω R16 resistor could be set to allow proper operation of the TDR unit for the particular circuit layout of Preisser-Mineco. A second necessary modification was the separate routing of TDR signal leads using 16 gauge lamp cord.

One prototype unit was found to have an intermittent open Z₀ adjust potentiometer, a malfunctioning 8601 IC, and an inconsistency of ground wiring in comparison with the other three prototype units. Because of the inconsistency in ground wiring the unit failed to operate properly.

The major reason for the failure of the prototype to operate properly was traced to ground noise pick-up resulting from printed circuit board layout and external wiring. To insure proper operation it is necessary to isolate the TDR signal leads from the remaining wiring. Considerable care must be given to the layout of all components in the vicinity of the 9615(U5) integrated circuit. All signal paths including those through trimpots should be kept as short as possible. A good ground bus should also be used to minimize voltage drops within the circuit.

The trimpots should be located near the component which they control and should not be brought out at the end of the board since this relocation will increase noise pick-up. The trimpots can be of the single turn cermet type.

The 9615 (U5) and MC4024 (U1) integrated circuits should be mounted in sockets to ease testing and aid in component replacement should these two devices be out of spec.