AVALANCHE PHOTOIONIZATION DETECTOR

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ABSTRACT

This paper reports a microfluidic gas sensor termed avalanche photoionization detector (APID). The APID employs miniaturized vacuum-UV (VUV) lamp as a photoionization source to ionize volatile organic compounds (VOCs) within a microfluidic ionization chamber made of a MgF_2 substrate bonded to an etch-through silicon microfluidic channel. The resultant electrons are collected by a reversely-biased avalanche P/N junction and subsequently undergo an avalanche process within the junction's depletion region, resulting in a substantial internal gain.

KEYWORDS

Microfluidic gas sensor, avalanche P/N junction

INTRODUCTION

Gas sensing is ubiquitous. There are many types of gas sensors. Among them, ion-based gas sensors are the most commonly used by virtue of their high sensitivity. An ion-based detector consists of an ionization source and an ion detector. Gas molecules are first ionized, and the resulting ions (positive/negative ions and electrons) are detected for analyte quantification. Ionization sources include flame ionization, photoionization (vacuum-UV light), and radiative materials (Nickel-63), *etc*. After ionization, the captured ions (or electrons) form an electrical current that is subsequently converted to voltage. State-of-the-art photoionization detectors (PID) [1, 2] can reach a sensitivity to the level of parts-per-trillion (ppt) for volatile organic compounds (VOCs). Traditional PIDs are Faraday cup based gas detectors and do not have internal gain. In contrast, an electron multiplier tube (EMT) [3] has large internal gain due to a series of voltage-biased dynodes. Consequently, EMT can count individual ions. However, an EMT requires high voltage (>1000 V) and vacuum to operate and it is also bulky and expensive. To achieve a higher detection capability (even down to single-ion level) in a portable instrument working in ambient environment, an alternative design is required.

In this report, a solid-state form of EMT using silicon based P/N junction, called avalanche photoionization detector (APID) is described. A reversed-biased P/N junction is embedded inside a microfluidic photoionization chamber to achieve avalanche amplification of the electrons produced by ionizing analyte molecules via impact ionization within the depletion region of the P/N junction [4]. An avalanche effect of the electrons is observed with an internal gain estimated to be from 10 to 400 in the linear mode (analogous to the terminology used in avalanche photodiodes (APD) [4]), and over 10^5 in the Geiger mode.

DESIGN AND WORKING PRINCIPLE

The device structure of APID is shown in Figure 1(A). It consists of an ionization source, an ionization chamber, electron/ion deflector/collector electrodes, and a semiconductor P/N junction that is reversely biased. The primary electrons (or negative ions) produced by gas molecule ionization are collected by electrodes driven by the bias voltage and then accelerated in the depletion region by the electric field of the reversely biased P/N junction to form avalanche electrons. Consequently, the signal (*i.e*., current) can be amplified via the internal avalanche process by impact ionization [4], which in turn, increases the APID sensitivity with the additional secondary electrons. A fabricated APID die is shown in Figure 1(B).

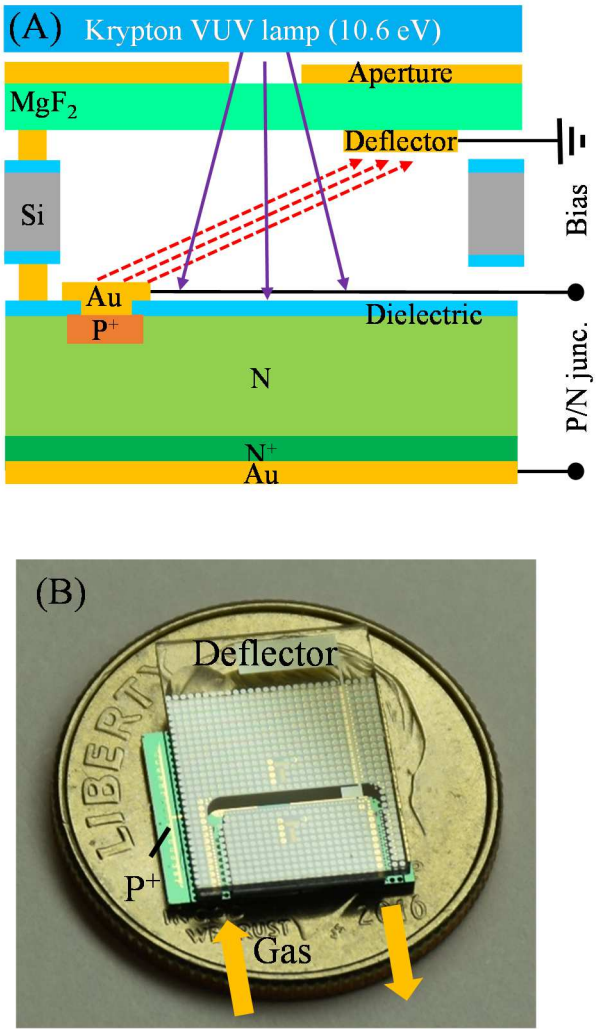

Figure 1: (A) Device architecture of an APID. Bias voltage is applied to deflect the electrons to P/N junction where the applied voltage is reversely biased to achieve the avalanche effect. VUV illumination (solid lines) is limited by the aperture patterned on top of a VUV transmissive MgF_2 window. Deflector electrode and P/N junction top contact are placed in an offset fashion to avoid contact with VUV photons. The collection field is indicated as dash lines. (B) Photograph of an APID die. The aperture is not patterned for clarity. N contact at the backside of the die.

Yellow arrows indicate the gas inlet and outlet.

FABRICATION

First, the avalanche P/N junction was made on wafer level. One side of the moderately doped N-type (phosphorous) silicon wafer (0.3-0.5 Ω*cm) is heavily doped with phosphorous for forming the ohmic contact with the metal layer at later stages. Thermal oxide was used as the diffusion mask in this step to reduce interfacial defect states. Phosphorous diffusion with a temperature of 950 °C for 2 hour was carried out. After diffusion, the mask oxide as well as the phosphorous silicate glass (PSG) were stripped by buffer hydrofluoric (BHF) wet etch. Then, the alignment marks used for lithography exposure using a stepper were etched by reactive ion etch (RIE) on the silicon substrate for 100 nm. Next, the P^+/N junction was formed. Thermal oxide can no longer be used due to the N^+ layer formed. Low pressure chemical vapor deposition (LPCVD) was used for growing 600 nm of high temperature oxide (HTO) with 900 °C for 1 h as mask oxide on the wafer. Next, a 15 µm circular opening defining the P^+ well was patterned and the mask oxide was dry-etched by RIE for 500 nm before BHF wet-etching the final 100 nm of mask oxide to protect the Si surface from RIE. The boron diffusion was carried out with 1000 °C for 2 hours to form a ~250 nm shallow junction. Note that the diffusion oxide mask was not applicable to be used as the self-aligned dielectric layer for metallization as the boron also has diffused into the oxide and a thin boron silica glass (BSG) layer was grown during diffusion. These would result in a high leakage current. After stripping mask oxide and boron silica glass (BSG), a 500 nm LPCVD HTO was grown, and wafers were immediately annealed in forming gas (5% H_2/95% N_2) in 450 °C for 4 hours to reduce interfacial trap states in dielectrics post LPCVD. After the backside oxide was fully stripped in BHF and a 5 µm circular opening was patterned in the middle of the P^+ well, the metallization was carried out by e-beam evaporation and lift-off process. A tri-layer metal stack of 10 nm Titanium (Ti)/30 nm Platinum (Pt)/500 nm Gold (Au) was deposited on top of P^+ well. The Pt layer serves as the diffusion barrier of gold to prevent potential leakage currents. On the other side (N^+), 10 nm Ti/500 nm Au stack was deposited without a barrier layer. It was experimentally found that a metal pad area on P^+ well larger than 1 mm resulted in leaky reverse bias current without an avalanche effect. This was hypothetically attributed to the fact that LPCVD SiO_2 had surface defect states and a larger contact could pick them up more easily than smaller pads. After dicing, this problem was resolved by depositing an additional layer of Al_2O_3 by atomic layer deposition (ALD) for surface passivation. The die then went through BHF patterned wet etch to expose the metal contact and followed by another layer of metallization where the metal pad area was extended.

Secondly, the APID was monolithically assembled through gold-gold thermocompression bonding of three layers: (1) avalanche P/N junction; (2) microfluidic channel; and (3) patterned MgF_2 window. The avalanche P/N junction was patterned with gold bonding dots, which were isolated from each other such that the any defective sites on dielectric can be localized. The first step was to bond an etch-through microfluidic chip which was made separately on another wafer. Two dies were bonded via gold-gold thermocompression bonding with conditions of 300 °C, 2 MPa for 30 minutes in ambient using a flip-chip bonder. The bonded pair was then diced along the edge of the microfluidic channel exposing its inlet and outlet. Subsequently, cold-welding was applied to bond the MgF_2 and bonded pair due to their large coefficient of thermal expansion mismatch. The temperature applied on the MgF_2 side was at 60 °C while Si at 150 °C with the same force (2 MPa) and a shorter time (10 minutes) in ambient.

EXPERIMENTAL RESULTS

A gas source with certain concentrations was introduced into the microfluidic chamber from the inlet, which was driven by a pump on the outlet. Helium with an ionization potential (24.6 eV) exceeding the VUV photons (10.6 eV) is introduced as the control "dark" current, as compared to the acetone (9.7 eV) which was selected as a representative analyte of VOCs. A bias voltage was fixed between the deflector and the P^+ terminal during the voltage scan of the P/N junction during the gas sensing.

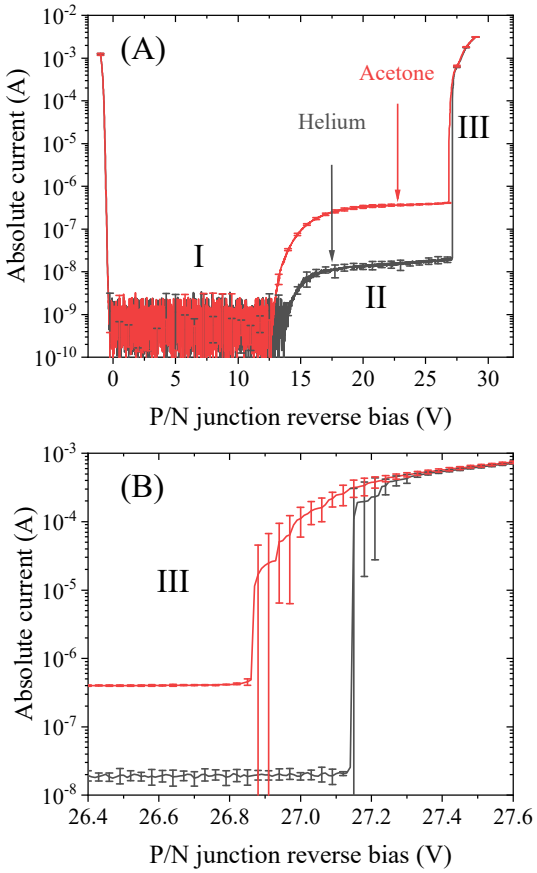

Figure 2: (A) Current-voltage (I-V) characteristics of the P/N junction in the AGID when the deflection bias voltage is fixed at 24 V. The microfluidic ionization chamber was filled with acetone (red curve, ionization potential (IP) = 9.7 eV); and helium (black curve, IP = 24.6 eV). Region I to III are indicated for different applied voltages. Acetone was sampled from the headspace of a vial containing acetone solution (density = 8 x 10^{21}/L). (B) Zoom-in view

for P/N junction reverse bias = 26.4 – 27.6 V.

I-V characteristics of the P/N junction of the APID are shown in Figure 2. Compared to the helium current, when acetone gas was introduced into the APID, an apparent additional current (red curve) was observed at the same reverse bias voltage in regions II to III. In region I (PN junction reverse bias = 0 to ~12.5 V), the acetone current was entirely buried inside the baseline noise floor (helium). When voltage was increased beyond region I, an initial avalanche feature was observed with acetone current rising above the background. The "turn-on" voltage also shifted to smaller voltages. Further, a four-order of magnitude increase of avalanched acetone current was observed when the reverse bias voltage was scanned near the breakdown voltage (region III) as shown in Figure 2(B).

DISCUSSION AND CONCLUSION

To quantify the avalanche current as well as the internal gain of the avalanche process, a net VOC current was calculated by subtracting the helium background current from the acetone current in Figure 2(A). Analogous to the treatment in an APD, the net current can be categorized into three regimes with respect to the P/N junction reverse bias voltage: (1) PIN mode, (2) Analog mode, and (3) Geiger mode, which correspond to the aforementioned region I to III, respectively. Gain can be therefore estimated by normalizing the signal to the PIN mode net current (~1 nA). Note that this value was on the same level as the noise, the gain was conservatively estimated using this method. As a result, for analog mode (region II), the gain ranges from 10 to 400. The APID is said to be operated in a linear amplification mode. The ionized electron would experience a linear amplification with certain gain depending on the reverse bias voltage. When operated in region III, the APID is operated at the so-called Geiger mode with an extremely high gain (~ 10^5). APID is operated in a binary detection mode (*i.e.*, counting mode) within this regime, which could be useful for detection of extremely low concentrations of gas.

In summary, this work presented a miniaturized MEMS-based microfluidic gas sensor consisting of an ionization chamber embedding an integrated avalanche P/N junction with an internal gain mechanism. Avalanched VOC current was observed with an internal amplification as high as 10^5.

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